Characterizing Distortion in Successive-Approximation Analog-to-Digital Converters due to Off-Chip Capacitors within the Voltage Reference Circuit

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The Successive Approximation Analog-to-Digital converter (SAR-ADC) is a popular architecture due to its low power, simple design, and reasonable resolution and speed. Due to the prevalence of ADCs in modern hardware, it is important to investigate opportunities to reduce the cost of the circuit without performance losses. One measure of the ADC's performance is its linearity. Linearity in the SAR-ADC is highly dependent on the linearity of its internal Digital-to-Analog converter (DAC). The DAC requires a reliable reference voltage in order to output the correct result. A band-gap reference circuit is generally used in low power applications such as ADCs. However, the reference circuit's stability is limited by the internal DAC's fast transient load. Large off-chip bypass capacitors are used to maintain a stable reference voltage. Investigating how the bypass capacitor can be moved on-chip will help provide a solution for reducing space and costs of the ADC due to non-integrated components.

The off-chip capacitance within the reference circuit was varied to create a characteristic curve showing how distortion is affected. Once a relationship was determined through measurements, a Matlab model was generated to simulate the observed behaviour. Through simulation and circuit analysis, a relationship between the input voltage, off-chip capacitance and the voltage reference perturbations was found. With this insight, the process of designing a fully integrated solution without losses in linearity can begin.

Acknowledgements

There are several people who have helped me through the last two years. Professor David Nairn, thank you for taking me on as your student and for being my mentor. My knowledge of in analog circuits grew exponentially with every meeting. I would like to thank Professor Opal and Professor Sachdev for taking the time to review my thesis. I would also like to thank all my MASc colleagues, especially Daniel Saari and Alireza, for always keeping me on my toes and motivating me to move beyond my own tasks. I would like to thank my best friends Krishna Moorthy, Vydehi Kamalanathan, Amar Nomani and Suk-Jin Kim for not only editing my thesis but also for always being there through all the stress. Lastly, I would like to thank my parents for all their love and support.

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List of Acronyms & Abbreviations

ADC	Analog-to-Digital Converter
C_a	The Array Capacitance
C_{bottom}	The total capacitance of the bottom capacitor array
C_{eq}	The equivalent input capacitance as seen by the reference
C_{ref}	The reference capacitor
C_{top}	The total capacitance of the top capacitor array
C_{unit}	The Unit Capacitance
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity Error
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
IC	Integrated Circuit
INL	Integram Non-Linearity Error
LSB	Least Significant Bit
MSB	Most Significant Bit
MSPS	Mega Samples Per Second
PCB	Printed Circuit Board
Q_{bottom}	The charge across C_{bottom}
Q_{top}	The charge across C_{top}
SAR	Successive Approximation Register
SAR-ADC	Successive Approximation Analog-to-Digital Converter
SFDR	Spurious-Free Dynamic Range
SHA	Sample and Hold
SNDR	Signal to Noise plus Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System-on-Chip
THD	Total Harmonic Distortion
V_{bottom}	The voltage across C_{bottom}
V_{error}	Voltage of the error
V_{FS}	Full-scale Voltage
V_{in}	The Input Voltage
V_{LSB}	Voltage of one LSB
V_{ref}	Voltage Across C_{ref}, also known as the Reference Voltage
V_{top}	The voltage across C_{top}

Chapter 1

Introduction

In the realm of mass produced analog circuits, a minor savings in space and production costs are significant to any designer. However, these savings are difficult to identify and require extensive research to achieve. Such savings can be found when interfacing and designing circuits that include analog to digital converters (ADC). Due to the prevalence of ADCs in modern hardware design, it is important to investigate these opportunities to save, especially within the University research setting. To a system level designer who requires an ADC, understanding the inner workings of the device is not significant. The goal is to interface with the ADC such that the output achieves the required specifications. This interface generally includes overly robust components that follow general circuit design guidelines. Without understanding how the ADC works, however, the interface will not be designed to push the boundary towards a truly cost-effective design. By characterizing how the components within this interface affect the output of the ADC, an optimally sized component can be identified. This allows for significant cost and space savings when working with printed circuit boards (PCB), but additionally within the realm of integrated circuits (IC). Of course, the investigation and research comes at the cost of the designer's time.

There are many types of ADCs for a designer to choose from. One such ADC is the Successive Approximation ADC (SAR-ADC). The SAR-ADC is designed to be low cost, relatively small in design, low-power, and precise [1]. The interface for the SAR-ADC is relatively simple; however it relies significantly on a stable reference voltage. The reference voltage is provided by another circuit known as the voltage reference circuit. Within the realm of PCBs, the reference circuit and the ADC are both embedded within their own separate integrated circuits. To meet stability and performance requirements a bypass capacitor is placed in-between the voltage reference and the SAR-ADC's reference voltage pin. The bypass capacitor is off-chip, and usually a surface mounted component on the PCB. By general ADC interfacing guidelines, the bypass capacitor is sized to be larger than required.

This consumes designer board space and results in an increase in component costs.

The purpose of this thesis is to characterize the effect of this off-chip bypass capacitance on the output performance of the Successive Approximation ADC. This will be done through experimentation on a real ADC to generate characteristic curves relating reference capacitance to several output specifications. Then using circuit analysis, mechanisms that shape the characteristic curves will be identified. This is an important step as it allows the findings of this thesis to be applied towards a variety of SAR-ADC architectures. The circuit analysis will then be used to generate a model through Matlab. Through Matlab, the model will be used to verify the lab measurements through a comparison with simulated results, and to gain further insight into the inner workings of the circuit. Once characterized, the purpose and size of the capacitor will be understood, such that a designer can optimally size the component.

Modern hardware design has been moving towards fully embedded solutions with all required components on-chip within a single system-on-chip (SoC). In a completely integrated design, silicon area is very valuable. Within a single IC, which includes a SAR-ADC structure and the voltage reference circuit, optimally sizing the bypass capacitor will allow for a reduction in the cost and size of the entire system.

1.1 Thesis Outline

This thesis is divided into three main chapters. Chapter 2 will review relevant data converter fundamentals, as well as details of successive approximation ADCs. The information presented is required to understand the analysis done in Chapter 3. In the third chapter, the non-ideal switching within the SAR-ADC will be analyzed. The purpose of this chapter is to create an understanding of how the distortion originates, and how it will be modeled. In chapter 4, real world measurements are taken as a reference. The apparatus and procedure of the experiment used to measure distortion caused by the off-chip bypass capacitance will be introduced. The data collected will presented, and used as a guideline for the next chapter's results. Chapter 5 contains results generated through simulation. It discusses the similarities and differences between the measured and simulated results. The thesis will end with a conclusion section, outlining key findings and presenting possible directions that this research can take in the future.

Chapter 2

Data Converter Fundamentals

The concepts covered in this chapter relate to data transmission in circuits. The two relevant forms of data transmission include analog transmission, or the transfer of data in a continuous time-varying domain, and digital data transmission. Analog signals are physical signals that represent phenomena in the real world. In electronics, analog signals exist as time-varying voltage levels that are generated by devices such as sensors or wireless receivers. They are also internally generated to control devices in the outside world, relative to the circuit. Examples of such devices are speakers, monitors and wireless transmitters. Digital signals are electronic signals used for digital signal processing. They are usually exist as two distinct voltage levels, and are interpreted as logic ones and zeros. A string of ones and zeros is known as a binary code. Digital signals are used internally within circuits, to communicate between the different digital, signal processing circuit blocks. Two popular devices that use digital signal processing are computers and cellphones. Most modern devices include circuits both types of data transmission. The next section will discuss common specifications that define analog and digital signals.

2.1 Analog and Digital Signals

Analog Signals are represented by a value within a finite voltage range. This is because the circuits involved are designed to read or output analog signals that are limited within this range. The maximum magnitude voltage is known as the full-scale voltage, or V_{FS}. A unipolar device uses signals that range from 0V to V_{FS}. These signals usually come from single-ended designs. Bipolar devices consider signals ranging from $-V_{FS}$ to $+V_{FS}$ and are used for differential circuits. Within this voltage range are an infinite amount of distinct voltage levels. For digital codes, however, there are a finite amount of possible values.

Digital signals are used for data processing and communication. Though they exist as voltage levels, they are interpreted in discrete-time. At every discrete time interval, the digital value is interpreted as a bit. These bits make up individual codes of a finite length N. Since digital codes are made up of zeros and ones, there are 2^N unique codes. One type of digital code is straight binary. Straight binary code defines each bit as powers of 2, with the least significant bit (LSB) being 2^0 or 1. Each subsequent bit is double the value of the latter. The most significant bit (MSB) represents a decimal value of $2^N - 1$. Thus, a straight binary digital code of length N can represent any decimal integer value between 0 and $2^N - 1$. Table 2.1.1 shows an example of how a 3-bit binary code can be interpreted as straight binary. The data converter is able to convert between analog and digital signals that meet the requirements of the discussed specifications.

Table 2.1.1: 3-Bit Code Interpretation in Straight and Fractional Binary

Code	Straight Binary	Fractional Binary
000	0	0/8
001	1	1/8
010	2	2/8
011	3	3/8
100	4	4/8
101	5	5/8
110	6	6/8
111	7	7/8

2.2 Data Converters

The data converter is a circuit or system that converts signals between the analog domain and the digital domain. The two data converters in electronics are the Analog-to-Digital converter (ADC) and the Digital-to-Analog converter (DAC). On the digital side, ADCs and DACs are constrained in the length of digital code which they can interpret. The value N represents the number of bits per code that the data converter works with, and is also known as the data converter's resolution. The resolution is determined by the ability to correctly divide or distinguish analog signals. Analog signals that the ADC and DAC correspondingly input and output are limited by V_{FS}. These data converters can be unipolar or bipolar. Figure 2.2.1 summarizes the input and output of DAC and ADC circuit blocks.

The DAC converts digital codes into analog voltages. Most DAC architectures can be

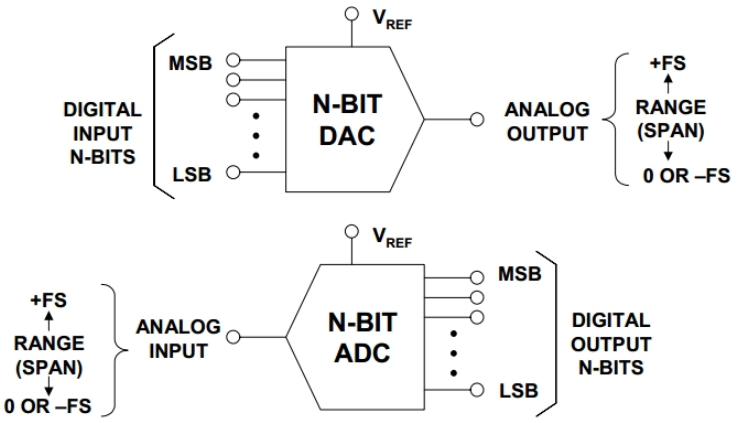


Figure 2.2.1: Summary of ADC and DAC Top Level Input and Output [2]

loosely described as an array of passive components connected together forming a closed circuit array with intermediate nodes. These intermediate nodes hold analog voltages that are unique and equally seperated voltages between 0V to V_{FS}. A switching network is then used to access intermediate nodes within the structure. Each digital code will control the switching network such that the DAC's output is a unique analog signal. If an N-bit digital code $(b_1b_2b_3...b_N)$ entering a DAC controls the switching circuit, then the output of the DAC can ideally be written as:

$$V_{out} = (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + ... + b_N 2^{-N}) * V_{FS} \tag{2.2.1}$$

It should be noted that in equation 2.2.1, each bit represents a fraction of V_{FS} at the output, rather than a decimal integer. This scheme is known as fractional binary, and is similar to straight binary as shown in Table 2.1.1. This is a good place to also define the term V_{LSB} or the voltage of the least significant bit (LSB). Since the Nth bit represents the LSB, from equation 2.2.1 above it can be deduced that:

$$V_{LSB} = \frac{V_{FS}}{2^{-N}} \tag{2.2.2}$$

ADCs are sometimes considered the inverse of the DAC due to their opposite purpose. Functionally, however, there are many key differences. While DACs are able to convert one unique digital code to one unique analog signal, each of the ADCs unique digital output codes corresponds to a range of possible analog inputs. This is because it cannot be assumed that the analog input will be in distinct steps, but rather exist within the full range 0V to V_{FS}. The ADC generally has a DAC, or DAC-like structure within its architecture. This is because an ADC can be loosely described as a system that takes in an analog input and searches

for a digital output that most closely describes it. This is done by generating several analog outputs from the DAC within it. Then comparing the output of the DAC to the analog input until a correct code is found. Keeping this structure in mind, the formula to model this, equation 2.2.3, shows a lot of resemblance to equation 2.2.1 above.

$$V_{FS} * (b_1 * 2^{-1} + b_2 * 2^{-2} + b_3 * 2^{-3} + \ + b_N * 2^{-N}) = V_{in} \pm V_{error} \tag{2.2.3}$$

The V_{error} term is known as the quantization error, and is a consequence of analog to digital conversion.

2.3 Quantization, Noise and Distortion

This section will discuss the non-ideal artifacts of analog to digital conversion. These non-ideal behaviours can be both an implicit result of the conversion, due to errors in the ADC or due to external sources.

2.3.1 Quantization

In the context of data converters, quantization is the process of mapping analog signals to digital codes. Figure 2.3.1 shows a quantization characteristic transfer curve that defines the mapping for a 3-bit ADC. To recover the analog signal, each digital code is translated into a discrete analog value. This can be seen in Figure 2.3.2.

For an ideal ADC, perfect quantization is very improbable. As seen from equation 2.2.3, quantizing an analog input also leaves a remnant error term known as the quantization error. Take for example an ideal unipolar ADC. The ADC takes an input between 0 and V_{FS} and converts it to the closest appropriate digital code. This digital code, however, describes a precise analog voltage that is not identical to the analog input. Thus, an infinite range of analog voltage signals quantize to the same digital code, and the probability of sampling the "correct" voltage is extremely low. The deviation from this voltage, the quantization error, always exists. This implies that there is information loss due to these errors during the quantization process. Figure 2.3.1 shows how a 3-bit analog code is quantized graphically. Additionally, an analog input exists in continuous time while digital signals are discrete. The ADC will take in input samples in discrete time intervals, and maintains that input for quantization even though the analog signals are continually changing. By the time the quantization process is complete, the output of the ADC no longer represents the input at that time. This error can be improved by increasing the sampling rate.

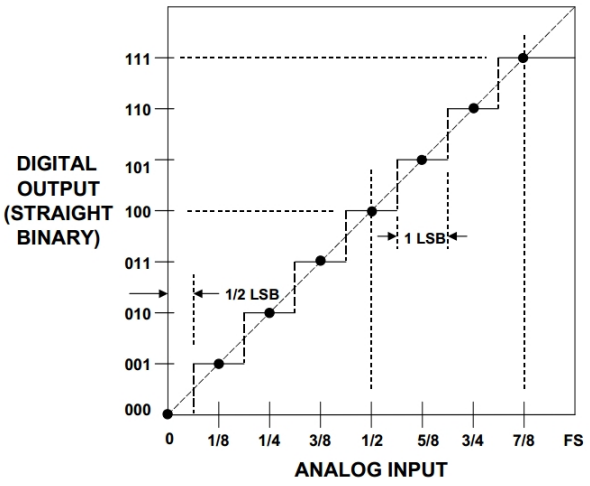


Figure 2.3.1: Input to Output Characteristic Transfer Curve for an Ideal ADC [2]

If the resolution of the ADC is increased, the magnitude of quantization error is decreased but never eliminated. Ideally the error associated with quantization is always limited to $\pm\frac{1}{2}V_{LSB}$. Its actual value can always be found if the input is known. Since the quantization error is input dependent and the possible analog inputs are infinite, the errors seen at the output begins to look random after several samples are taken. This random error looks like noise in the frequency spectrum, hence it is also known as quantization noise.

Unlike ADCs, an ideal unipolar DAC translates digital code into an appropriate analog voltage level. Though there are an infinite possible number of voltage levels between 0 and V_{FS}, the ideal DAC's analog output is limited by its design. Hence, it has the same number of unique outputs as it does inputs. Figure 2.3.2 outlines how a 3-bit DAC maps digital codes into distinct analog levels.

2.3.2 Noise

In the real world, data converters never achieve ideal quantization. There always exists non-ideal behaviour, tolerances in component values, internal and external noise sources that all lead to two types of errors at the output. These two types of errors are distortion and noise. This noise is not to be confused with quantization noise. Quantization noise always exists within the ADC structure, even in ideal models as previously explained. Noise is randomly generated internally, but also can come externally through a device's inputs. Possible noise sources are thermal noise and flicker noise.

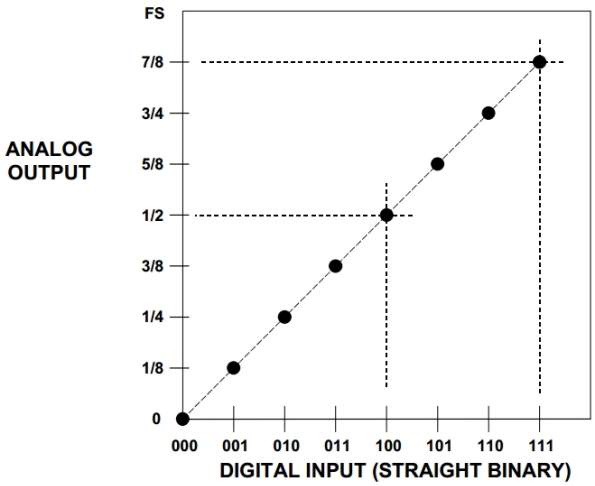
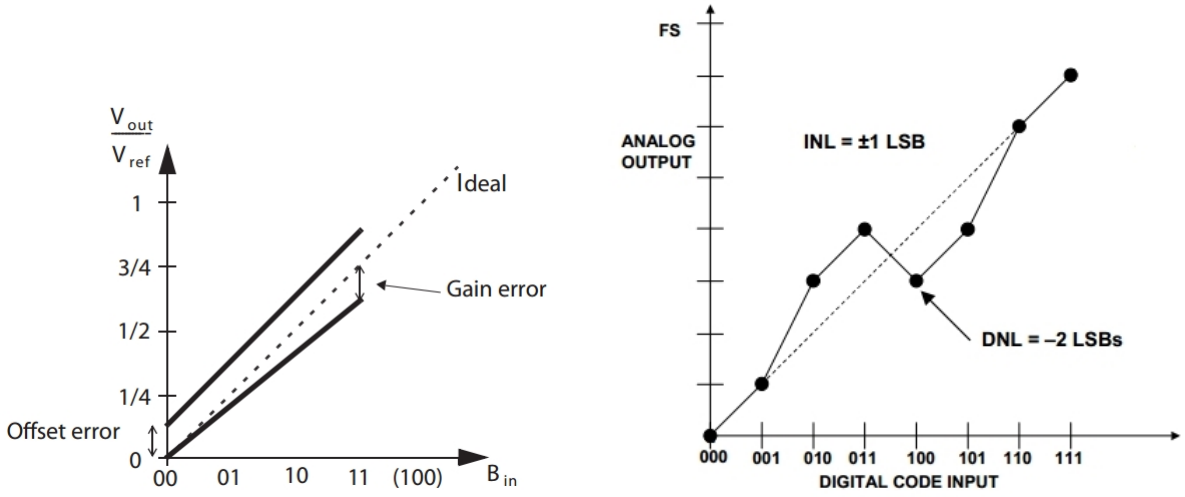


Figure 2.3.2: Input to Output Characteristic Transfer Curve for an Ideal DAC [2]

2.3.3 Distortion

This thesis, however, is primarily concerned about distortion. Distortion in data converters refers to the phenomena when the ADC or DAC cannot return the ideal output regardless of noise. This incorrect quantization is not random, but instead is caused by non-ideal behaviours of the data converter architecture. The most basic of these errors are linear errors, or more specifically, gain and offset errors. For a DAC, an offset error occurs when the analog output is not 0V for a zero digital code. Gain error is the deviation from the output's full-scale voltage after taking account of any offset errors [3]. These two errors are illustrated graphically in Figure 2.3.3a. For an ADC, linear errors are similarly defined. However, both these errors do not hold much significance to this research as they can be corrected during post simulation/measurement analysis.



(a) Linear Error

(b) Non-Linear Error

Figure 2.3.3: Transfer Curves with Linear and Non-Linear Errors [3] [4]

The more significant errors are known as non-linear errors. After linear errors are corrected, the remaining errors that exist contribute to the data-converter's non-linear error [3]. An example of non-linear error can be seen in Figure 2.3.3b. For a DAC, non-linear errors may imply inconsistent voltage steps between adjacent codes. A significant issue is with monotonicity, or if the analog output of code is lower than the previous code. Similarly, an ADC can be non-monotonic if the digital output code decreases for an increasing analog input. Another non-linear error in ADCs are missing codes, or when specific digital codes are skipped and will never show up at the output. Learning how non-linear distortion is measured will provide important insight into the different issues that it causes.

2.4 Specifications and Measurements

It is important to note that the Successive Approximation ADC has a DAC structure within it, as will be discussed in Section 2.5.3. This DAC structure can have non-linearity associated with it that leads to non-linearity at the output of the SAR-ADC. The internal DAC's errors cannot be measured, but the non-linear behaviour it causes at the final output of the ADC can be. Since this report is focused on the Successive Approximation ADCs, the content of this section will focus on the measuring of non-linearity of ADCs.

2.4.1 Static Testing

Looking at the non-linear characteristic curve of an ADC in Figure 2.3.3b, the amount of non-linearity can be measured by comparing the range of analog inputs between digital transitions. In the ideal case, every transition should be seperated by V_{LSB}, or 1 LSB. The Differential Non-Linearity Error (DNL) is defined as the largest deviation from the ideal 1 LSB out of all the transitions [2]. For an ideal ADC the DNL error should be 0 LSB. If an ADC's DNL measures 0.5 LSB, this implies that the length of analog signals per digital code can range from 0.5 LSB to 1.5 LSB. However, knowing the transition lengths does not say anything about the worst case error. Another measurement to characterize non-linearity is to compare each transition point to that of the ideal case. This measurement is known as Integral Non-Linearity Error (INL), and it is the largest error deviation from the ideal straight line [3]. DNL and INL measurements, as well as gain and offset errors, are part of static ADC testing. Static testing is usually done by applying a ramp to the input of the ADC and creating a characteristic curve from the outputs. The other way of testing the ADC is to apply a sine wave at the input. Then by creating a histogram which counts how many times each code is seen at the output. From this, the static measurements can also be taken. The sinusoidal signal is also used for ADC dynamic testing.

2.4.2 Dynamic Testing

Dynamic testing of an ADC is done through the input of a sinusoidal signal and inspecting the output in the frequency domain. Dynamic testing analyses the AC performance of the ADC by reconstructing digital output into an output sinusoidal signal. Due to non-linearities in the transfer curve of the ADC, the output sinusoid will be distorted and noisy. This new reconstructed output signal is put through a Discrete Fourier Transform. The algorithm to do this is known as the Fast Fourier Transform (FFT). The FFT takes in a finite number of samples from the output and then seperates them into sinusoids that are equally spaced by frequency. These sinusoids are ordered by finite frequencies, where frequency in the FFT plot is known as a FFT "bin". Under ideal conditions, when an ideal input sinusoids is sampled using an ideal ADC, the FFT will contain one large signal in the bin of the input frequency. Additionally, all other bins will contain significantly lower magnitude signals representing the quantization noise that has spread across the spectrum. In the non-ideal case as previously discussed, the FFT shows signs of additional noise and distortion. Noise is visible through the level the noise floor if the noise floor is at a higher level than that of quantization noise. Distortion is visible in the FFT through visible signals other than that of the input signal. These additional "spikes" are generally caused by harmonic distortion. Harmonic distortion implies the presence of harmonics, which are signals that are in frequencies that are integer

multiples of the fundamental input frequency. For example, the second harmonic can be seen in the bin that is twice the frequency of the input.

While Static testing provides information on how the ADC maps specific inputs to the digital outputs, Dynamic testing provides understanding to how the ADC will perform with a full-scale, time varying signal. This is important for digital communication applications. Dynamic specifications are used to quantify the noise and distortion with respect to a sinusoidal signal. These measures are SNR, SNDR, SFDR, and THD. Table 2.4.1 shows these measures and their definitions. They will be measured and calculated to analyze distortion in later chapters.

These dynamic specifications are important to define since measurements taken from different sources must be compared justly. The Signal to Noise Ratio (SNR) is the ratio of the signal amplitude to the root-mean-square sum of all the other components of the FFT, except for the first 5 harmonics and the DC term [5]. For this thesis, the Total Harmonic Distortion (THD) is simply the root-mean-square sum of the first 5 harmonics. The Signal to Noise plus Distortion Ratio (SNDR) is the ratio of the signal's amplitude to the root-mean-square sum of all spectral components include the harmonics [5]. Lastly, the Spurious-Free Dynamic Range (SFDR) is the ratio of the signal amplitude to the amplitude of the largest spectral component in the FFT [5]. All these terms will be converted and used as decibels (dB). Further details on how these specifications are calculated can be found in Section 5.2.2 in Chapter 5.

Table 2.4.1: Noise and Distortion Measurements for an ADC's Dynamic Performance

Specification	Definition
SNR	The Signal to Noise Ratio
SNDR	The Signal to Noise plus Distortion Ratio
SFDR	Spurious-Free Dynamic Range
THD	Total Harmonic Distortion

2.5 The Successive Approximation ADC

When the ADC samples an analog input, it "searches" for the appropriate digital output. The Successive Approximation ADC (SAR-ADC) uses a binary search algorithm to resolve the correct output. Because the binary search algorithm is the most efficient when dealing with sorted lists, the SAR-ADC has the lowest power consumption compared to other ADCs.

Additionally, it requires minimal components which makes the SAR-ADC cost effective in terms of price and space. This thesis is concerned with modelling distortion caused by the real capacitors within the SAR-ADC and voltage reference circuit. This section will provide an overview of SAR-ADC's workings and architecture.

2.5.1 Algorithm - Binary Search

An ADC quantizes an analog voltage by searching for the appropriate digital value. The SAR-ADC does so by following a binary search algorithm. If the resolution of the ADC is N, then it will take N iterations to successfully determine the correct code. The algorithm begins by taking in an analog voltage sample, and an initial code of 0. Then it will systematically turn a bit to 1, starting with the MSB. After switching the largest undetermined bit to 1, this new internal code is compared with the input. If this signal is larger than the input sample, then the bit is returned to 0. the bit will otherwise be resolved as a 1. This process continues to the next significant bit until all bits in the code have been resolved. Since the algorithm starts with the MSB and works its way down, the possible outputs are halved every time a correct bit is determined. This is as expected in a binary search.

2.5.2 Architecture

The architecture of the SAR-ADC is simple, requires low power, and has reasonably fast conversion times [1]. The main circuit blocks in the architecture that concern this thesis are the sample and hold (SHA), comparator, successive approximation register (SAR), the voltage reference circuit and DAC. A simplified overview of the structure is shown in Figure 2.5.1.

The SHA takes a sample of the input analog signal. It holds this voltage for the duration of the quantization sequence. The duration and timing for the sampling and quantization process are controlled by the timing and logic circuits. For the purpose of the analysis, the SHA will be considered ideal.

The comparator looks at the output of the DAC and SHA. The comparator circuit can determine if one signal is larger than the other and correspondingly provide an appropriate output. The comparator is usually a higher resolution than the ADC itself. Any distortion caused by this high resolution comparator will be smaller in comparison to other distortion sources. In this analysis, this analog circuit will also be considered ideal. The output of the comparator is used by the control logic to update the SAR.

The SAR keeps track of the digital code used in the binary search behaviour. It is part of a logic block. This logic block, in coordination with the timing block, controls the SAR-ADC

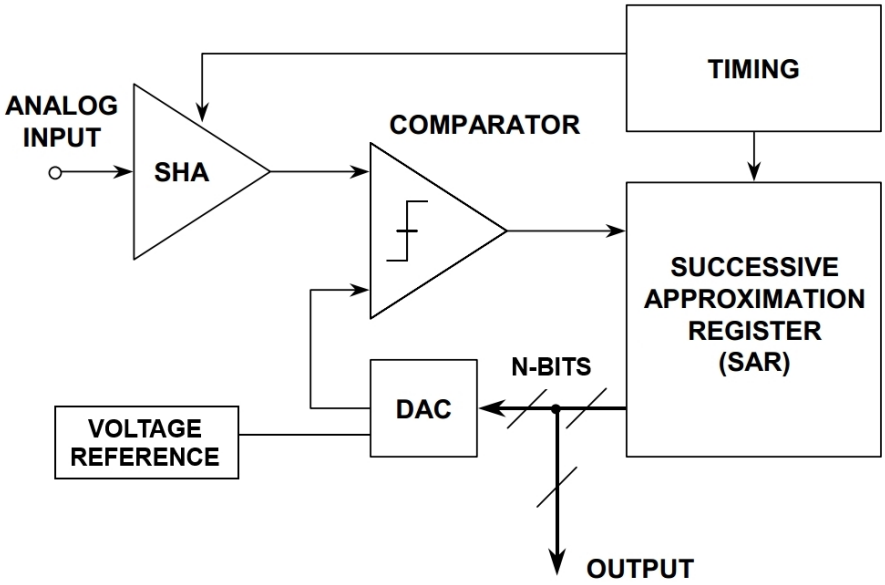


Figure 2.5.1: Basic Successive Aprroximation ADC Structure [1]

to follow the binary search algorithm. The control logic stored in the control circuit block looks at the output of the comparator and determines whether the bit in question remains high or is returned back to 0. At the end of N-iterations, the SAR holds the correct digital output for the ADC.

The voltage reference circuit is used to provide the full scale voltage, V_{FS} to the ADC. It is an analog circuit, which cannot be modelled as an ideal source. When connected to the ADC's non-ideal internal DAC, the voltage reference shows errors in the form of perturbations at its output. These errors will be investigated later in this chapter.

The DAC is the most significant circuit block with regards to this thesis. Its purpose is to take a digital input from the SAR and produce its corresponding analog output signal, which is then compared with the ADC's input analog sample. Along with the voltage reference, the internal DAC is a non-ideal analog circuit. The distortion due to the non-ideal circuit will begin with an investigation into how the circuit is constructed. For the purpose of this thesis, a simplified structure known as a charge sharing, or switch-capacitor DAC will be considered.

2.5.3 Binary Weighted Switched Capacitor DAC

The analysis in this thesis was done with the purpose of adding complexity only where completely necessary to model the non-ideal occurrences. The internal DAC, and its interaction with the voltage reference circuit, is the primary source of distortion being investigated. The

DAC pulls current from the voltage reference circuit, which is used to generate an analog output which maps to the digital input of the SAR. The magnitude of this current is independent of the internal structure of the DAC. A standard successive-approximation ADC, the internal DAC is used to compare an unknown analog signal to a voltage generated through binarily-weighted bit currents [6]. These currents are dependent on the total input impedance, but the capacitance can be set to any required value regardless of the structure. Because of this, complexity is not needed when deciding which DAC structure to use.

The most simple structure for a DAC is to use an array of capacitors, organized in a binary weighted array. The reason why an array of capacitors is used is because it is stated that the SAR-ADC uses a charge redistribution, or charge sharing, DAC [7]. These capacitors form a simple voltage divider. By switching capacitors on and off, the voltage division function can be accurately controlled. Since the switching is controlled by a digital signal which in turn leads to a unique analog output, the structure is considered to be a simple DAC. There are many ways to organize these capacitors, one of which is in a binary weighted array.

The binary weighted charge sharing DAC contains an array of N capacitors. Each capacitor is twice the size of the previous. Each switch controlling a capacitor in the array is controlled by the corresponding bit of code stored in the SAR. Thus, the most significant bit of the code corresponds to $V_{FS}/2$ at the output of the capacitor array. Similarly, the least significant bit corresponds to V_{LSB} at the output of the capacitor array. Figure 2.5.2 below shows the binary weighted array.

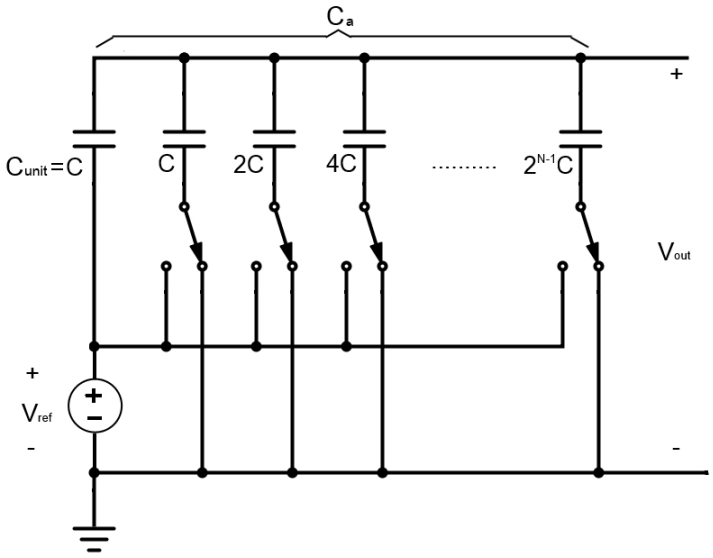


Figure 2.5.2: Binary Weighted Capacitor Array for a Charge Sharing DAC

The binary weighted charge redistribution DAC is not practical and probably not used in practice. One reason for this is the difficulty of fabricating a large array of matched

capacitors. When designing a high resolution SAR-ADC, the total capacitance increases exponentially with the number of bits [8]. With a large number of capacitors, the highly probably mismatch implicit within the internal DAC will cause distortion [8]. However, this thesis is only considering an ideal binary weighted DAC for simulation purposes.

The analog output of the DAC can be found easily. The capacitors that are switched on are connected between the reference voltage and the input of the comparator. The capacitors which remain off are between the comparator and ground. This implies that these sets of capacitors are in series. The output is a result of a voltage division between the capacitors that are turned on, and the ones that are turned off. The analog output resembles that of the fractional binary scheme. For example, if the largest capacitor is turned on, since it is equivalent to half the capacitance in the array, after voltage division the output is half of V_{ref}. This can be compared to the 3-bit code seen in Table 2.0.1, with the code 100. Further analysis of how the output voltage is determined is shown in the next chapter. The output of the DAC is compared to the input of the ADC. The result of this comparison controls how the SAR will be updated. However, the comparison is only valid if V_{ref} is equal to V_{FS}. Thus, it is important to provide an accurate reference signal. This is done through a voltage reference circuit.

2.6 Voltage Reference Circuit and Bypass Capacitor

The purpose of the voltage reference circuit is simple: provide V_{ref} to the ADC. In circuit theory it is typical to substitute this circuit with the ideal voltage source, then ignore the real effects it can have on the rest of the circuit. Voltage references have a significant impact on the accuracy of the ADC [9]. The dynamic load of the ADC can cause the output voltage of the reference circuit to change, which will be analyzed in Chapter 3. A 12-bit system with a 2V reference can handle a $\pm 0.5mV$ tolerance in V_{ref} before losing the required accuracy. Another determinant of the performance of the reference circuit is its handling of noise and short-term stability [9].

The SAR-ADC requires a reference that uses low power. This implies low bandwidth and output buffer amplifiers. The voltage reference circuit used for this thesis is known as a bandgap reference. The bandgap reference is used in many ADCs and DACs due to the fact that it operates at low voltages and has good long-term stability [9]. the SAR-ADC's fast transient load causes the reference to perform poorly [9]. The switching of the capacitors within the internal DAC cause its input impedance to change, which leads it to be considered a transient load. To deal with the high-frequency perturbations in the reference, a bypass capacitor is placed in between the reference and the SAR-ADC.

The bypass capacitor stores charge within it. When a change occurs that warrants a voltage drop, charge will get released from the bypass capacitor instead of from the reference circuit [10]. This maintains the reference voltage within the required tolerance. Like the non-ideal voltage reference circuit, the bypass capacitor is not an ideal capacitor. The equivalent circuit of the bypass capacitor is shown in Figure 2.6.1. The leakage resistance is generally high but it represents the fact that the capacitor will slowly lose charge and is not a perfect open circuit in its steady state. Two parasitic components are shown, which are the equivalent series resistance and inductance, or ESR and ESL. ESR leads to a small voltage drop during the discharge of the capacitor, and additionally leads to the production of heat. It is reduced by reducing the wiring connected to the capacitor. ESL, along with the equivalent resistance of the circuit, impacts the rate at which current can be discharged. ESL is controlled by the type and package size of the capacitor [10].

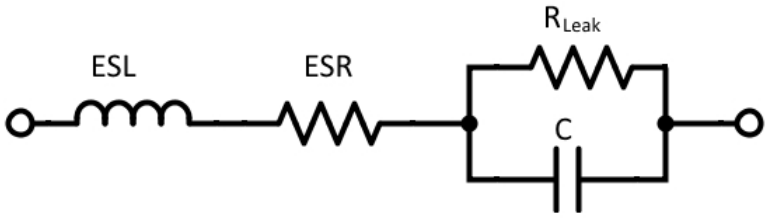


Figure 2.6.1: Equivalent Circuit for a Real Capacitor

It is clear that the size of the capacitor is directly proportional to the amount of charge it can store. The requirements of the SAR-ADC leads to a large, off-chip bypass capacitor to be used. The smaller the bypass capacitor, the smaller its effect on reducing voltage perturbations seen in V_{ref}. High-resolution digital signal processing applications preferably require on-chip data converters, which need sufficient decoupling [11]. The purpose of this thesis is to investigate what size bypass capacitor is required to maintain 12-bit accuracy, and to determine if the capacitance can be moved on-chip.

The key limiting factor of a well designed SAR-ADC is in its analog circuitry, which is the voltage reference circuit and the internal DAC. The interaction between these two circuits lead to the non-linear distortions described in this chapter. The next chapter will present an analysis used to determine a relationship between the voltage perturbations in V_{ref} to the switching of the capacitors within SAR-ADC's internal DAC.

Chapter 3

Analysis and Matlab Modelling

3.1 Introduction

The physical structure of a successive approximation ADC has been described in the previous chapter. In this chapter, the process of converting the functionality of the successive approximation ADC into a Matlab model will be investigated. With a Matlab model, errors and distortion caused by non-ideal circuitry can be isolated, measured and analyzed. By adding the non-ideal switching to an ideal ADC model, the distortion component due to a finite reference capacitance can be properly characterized.

3.1.1 The Ideal Successive Approximation Algorithm

The comparator and the Successive Approximation Register (SAR) work together to make a binary search algorithm. On one side of the comparator is the analog input. On the other side is the output of the DAC. The SAR then takes the output of the comparator to adjust the digital signal stored in its register. The SAR switches capacitors on and off in N iterations as it determines the value of all N bits to complete the binary search. At the end of the process, the output of the ADC should have a maximum error of 1 LSB. Regardless of how the hardware works, for modelling purposes the expected functionality is that when the SAR stores the code 0 (000000000000) the DAC output should be 0V. Similarly, when the SAR stores $2^N - 1$ (111111111111) the DAC output should be at its full-scale voltage. All other codes result in voltages in between full-scale and ground, which are adjacently separated by equal step increments. If the least significant bit is the right most bit, or Nth bit, then the digital code representing 1 represents a voltage at the output of $V_{ref}/2^N$. This voltage is known as V_{LSB}, and is the size of the step between the voltage outputs of adjacent codes.

Thus, ideally V_{out} is simply the code stored in the SAR multiplied by V_{LSB}. Then, the SAR will reset for the next sample. The Matlab code modelling this ideal behaviour is simply modelled by a for loop and if statement as seen below.

```
N=12                          %12-bit resolution
b = zeros(1:N)                %initialize the code stored in the SAR
Vref = 1                      %Reference is 1 Volt
VLSB = Vref/2^N               %Calculate V_LSB
for i=1:12                    %Begin algorithm
    b(i) = 1;
    Vdac = bin2dec(b)*VLSB;   %bin2dec converts binary to decimal
                              %Output of the DAC is Vdac
    if vin < Vdac             %SAR is updated based on the comparator
        b(i)=0;
        %else b(i) stays as 1;
    end

end                           %b stores the digital output
```

Figure 3.1.1: Matlab Code for an Ideal Successive Approximation ADC

Together this code implements an ideal ADC. When putting an ideal tone into this ADC it results in the following FFT:

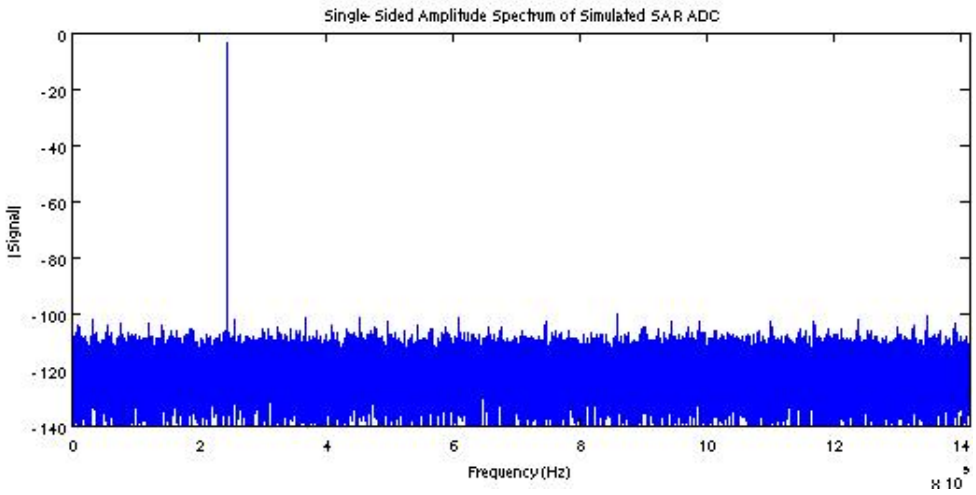


Figure 3.1.2: FFT Response from a Simulated Ideal ADC

This FFT plot shows the ideal result of a 12-bit ADC, proving that the correctness of the above algorithm. The next section will investigate how to include the non-ideal switching

behaviour from inside the charge sharing DAC. The resultant FFT should show signs of distortion. This distortion will be solely caused by switching since, as shown above, the rest of the code is ideal.

3.2 Analysis of Off-Chip Capacitance and Distortion

There are many ways to implement a charge redistribution DAC. However, to model a DAC for the purpose of this investigation, the common binary weighted DAC will be used. The capacitor array to be analysed is shown in Figure 3.2.1 below. All capacitors used in the array are ideal and have no tolerances associated with them. There will also be no redundancy or special power saving switching techniques incorporated into the logic. Another assumption used is that all switching required per iteration occurs instantaneously and at the same time. These switches are designed for proper settling and have small enough impedance to be neglected.

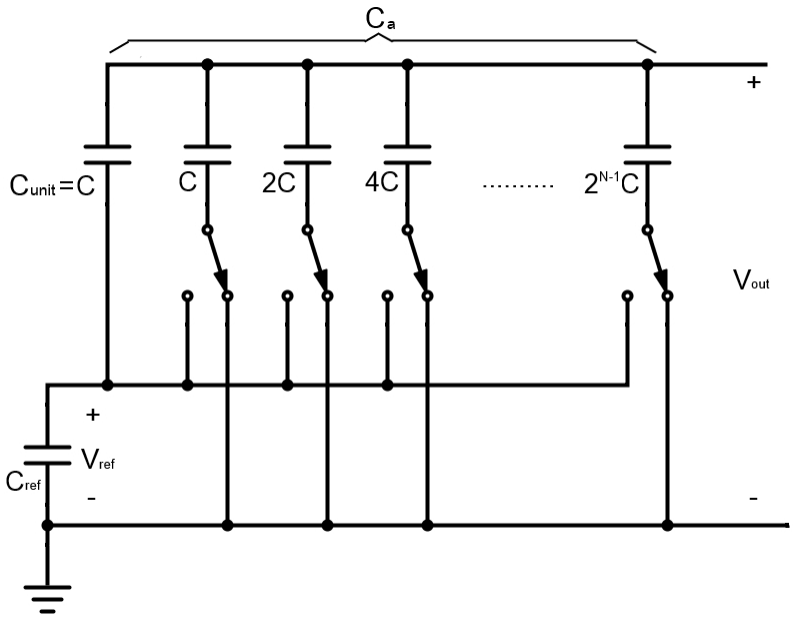


Figure 3.2.1: A charge sharing DAC's binary weighted switch capacitor array

The term C_{unit} represents the smallest capacitor used in the array; it is also known as the unit capacitance. All the capacitors within the binary weighted internal DAC are sized to be multiples of C_{unit}. The total array capacitance C_a is defined as the sum of all DAC's capacitors in a parallel array. It is also the maximum input capacitance seen looking into the DAC from the input of the reference voltage. Figure 3.2.1 differs from Figure 2.5.2 from Chapter 2 in that the ideal source V_{ref} is replaced by a capacitor, C_{ref}. In this thesis,

C_{ref} is referred to the reference capacitance since it holds the voltage V_{ref}. It represents the equivalent circuit representation of the off-chip bypass capacitor and voltage reference circuit. Both of these components are external to the ADC. The reason why the complex reference circuit and bypass capacitor is represented by C_{ref} can be found in Section 3.3 of this chapter. Typically, C_{ref} is significantly larger than C_a.

$$C_a = C_{unit} + \sum_{i=0}^{N-1} 2^i \cdot C_{unit} = 2^N \cdot C_{unit} \tag{3.2.1}$$

3.2.1 Modelling the Non-Ideal Reference Capacitor

In the successive approximation ADC, the switching sequence is controlled by a binary code b of length N. The code b can be represented as $b_1 b_2 b_3 ... b_N$ where b_i represents the ith bit in code. The switch capacitors in the charge redistribution DAC will undergo N switching cycles. With the first iteration, the most significant bit (MSB) in b will be set to 1. Then the b is converted into an analog signal through a DAC, and compared to the input signal. Depending on the comparison, the MSB is left as 1 or returned back to 0 as per a binary search. Now consider that the only non-ideal component in the model of the successive approximation ADC is that the reference capacitor, C_{ref}, meaning it has a finite capacitance. C_{ref} stores V_{ref}, and due to inductance, fast switching speed, and high impedance in the input line, it will be assumed that C_{ref} will not receive any more charge from an external source until a sample is converted. Thus, any charge pulled off of C_{ref} will decrease V_{ref} as per the relationship $V = \frac{Q}{C}$.

To model how V_{ref} is affected per iteration of the entire sampling process, the problem needs to be simplified to promote understanding and aid the analysis. The system can be redrawn as shown in Figure 3.2.2, which groups all capacitors connected to the reference voltage and those connected to ground.

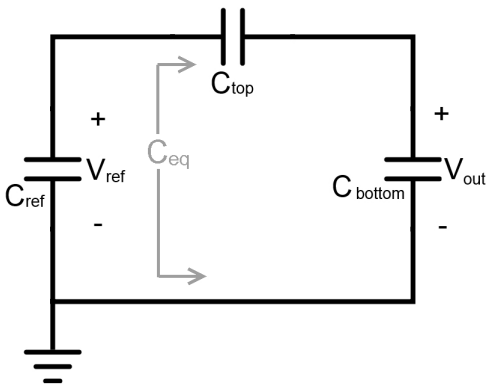


Figure 3.2.2: A simplified circuit representing the DAC's capacitor array

3.2.2 The Exact Model

The equivalent input capacitance seen by C_{ref} is two capacitors connected in series. The two capacitors are C_{top} and C_{bottom}, which are known fractions of C_a. Figure 3.2.3 shows the same circuit with new definitions for the capacitances shown. The new C_{eq} is now expressed in a more useful form shown in Equation 3.2.2.

$$C_{eq} = \left[\frac{1}{xC_a} + \frac{1}{(1-x)C_a}\right]^{-1} = x(1-x)C_a \tag{3.2.2}$$

The new variable x is defined below. It represents the fraction of capacitors turned on as defined by b. x ranges from 0 to $1 - \frac{1}{2^N}$. With this definition, Figure 3.2.2 can be redrawn as shown in Figure 3.2.3.

$$x = \sum_{i=1}^{N} \frac{b_i}{2^i} \tag{3.2.3}$$

It is also possible to find the charge held by each capacitor in terms of x, V_{ref} and C_a. By voltage division of series capacitors:

$$V_{top} = V_{ref} - V_{out} = (1-x)V_{ref} \tag{3.2.4}$$

$$V_{bottom} = V_{out} = xV_{ref} \tag{3.2.5}$$

The charge held by a capacitor is its capacitance multiplied by the voltage across it, thus:

$$Q_{top} = x(1-x)C_aV_{ref} \tag{3.2.6}$$

$$Q_{bottom} = (1-x)xC_aV_{ref} \tag{3.2.7}$$

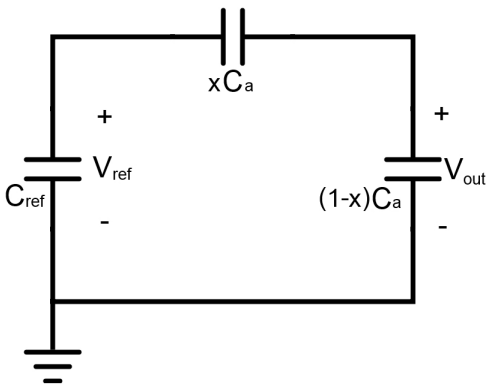


Figure 3.2.3: New definitions for the capacitances C_{top} and C_{bottom}

It is important to note that at this point, prior to switching, the charge across both capacitors are the same.

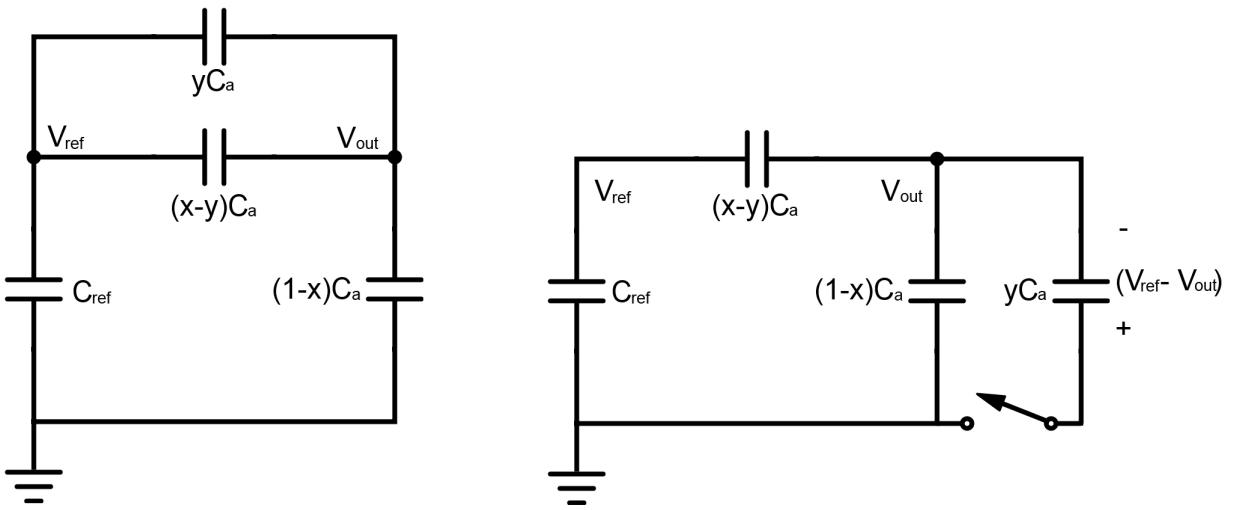
After the code stored in the SAR is adjusted, switching occurs instantaneously thus changing the values of the total top and bottom capacitances. Two types of switching occur per iteration, capacitors will switch from top to bottom and then also from bottom to top. To model the switching of the capacitors from top to bottom, the variable y is defined. y is defined similarly to x. It represents the fraction of capacitors moving from top to bottom as per which bits in b stored in the SAR are changing from 1 to 0. Figure 3.2.4 outlines how the capacitors are moving. After the y switching event, V_{out} changes. Let V'_{out} be the new value of V_{out}. The new voltage and charge is divided as follows:

$$V_{top} = (1 - x + y)V_{ref} = V_{ref} - V'_{out} \tag{3.2.8}$$

$$V_{bottom} = (x - y)V_{ref} = V'_{out} \tag{3.2.9}$$

The charge originally held by the y capacitors are $(V_{ref} - Vout)yC$. When these capacitors are moved from top to bottom, charge is redistributed and voltages are adjusted. Normally the reference capacitance C_{ref} is sufficiently large enough to maintain a constant V_{ref}. However, as C_{ref} becomes comparable to the capacitance in the DAC, V_{ref} decreases as charge is pulled off from C_{ref}. This is modelled by Equation 3.2.10 below. Note that V'_{out} is the new value of V_{out}.

$$V_{out}\left((1-x)C_a + \frac{(x-y)C_aC_{ref}}{(x-y)C_a + C_{ref}}\right) - (V_{ref} - V_{out})yC_a = V'_{out}\left(\frac{(x-y)C_aC_{ref}}{(x-y)C_a + C_{ref}} + (1-x+y)C_a\right) \tag{3.2.10}$$



(a) Initial

(b) After switching

Figure 3.2.4: The y switching sequence

$$V'_{out} = \frac{V_{out}\left((1-x)C_a + \frac{(x-y)C_aC_{ref}}{(x-y)C_a+C_{ref}}\right) - (V_{ref} - V_{out})yC_a}{\left(\frac{(x-y)C_aC_{ref}}{(x-y)C_a+C_{ref}} + (1-x+y)C_a\right)} \tag{3.2.11}$$

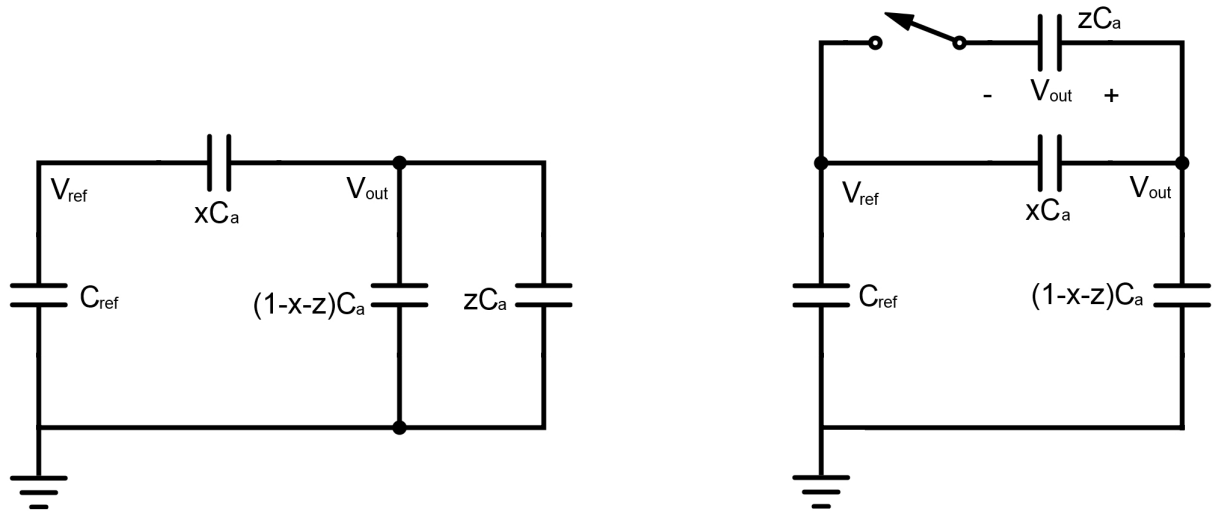
$$\Delta V_{out} = V_{out} - V'_{out} \tag{3.2.12}$$

Now that the change in V_{out} is known, the change in V_{ref} can be found using a simple voltage divider formed by C_{ref} and $(x-y)C_a$.

$$\Delta V_{ref,y} = \Delta V_{out}\frac{(x-y)C_a}{C_{ref} + (x-y)C_a} \tag{3.2.13}$$

From Equation 3.2.13, changes in V_{ref} are dependent on three important factors. Firstly, there is a clear dependence on the initial state of the capacitor array as defined by x. Secondly, it depends on the size of the capacitance being switched as defined by y. Thus, the change in V_{ref} is code dependent, since x and y values are dependent on the digital code being converted by the DAC. Lastly, there is also a clear dependence on the relative size of C_{ref} to C_a. Mathematically if the ratio of the capacitances approach infinity, it can be found that V_{ref} does not change.

The second case to investigate is the switching of capacitors from the bottom array to the top. Similarly to how y is defined, the variable z is now defined to identify the capacitance being switched in this case. A similar analysis is done to model how V_{ref} is affected by the switching. It is assumed that the z switching sequence occurs after the y switching sequence, so an intermediate x' is defined to simplify the analysis.



(a) Initial

(b) After switching

Figure 3.2.5: The z switching sequence

$$x' = x - y \tag{3.2.14}$$

$$V_{out} = xV_{ref} \tag{3.2.15}$$

$$\begin{aligned}(V_{ref} - V_{out})\left((x'C_a + \frac{(1-x'-z)C_aC_{ref}}{C_{ref}+(1-x'-z)C_a}\right) - V_{out}zC_a \\ = (V'_{ref} - V'_{out})\left((x'+z)C_a + \frac{(1-x'-z)C_aC_{ref}}{C_{ref}+(1-x'-z)C_a}\right)\end{aligned} \tag{3.2.16}$$

$$(V'_{ref} - V'_{out}) = \left[\frac{(V_{ref} - V_{out})\left(x'C_a + \frac{(1-x'-z)C_aC_{ref}}{C_{ref}+(1-x'-z)C_a}\right) - V_{out}zC_a}{(x'+z)C_a + \left(\frac{(1-x'-z)C_aC_{ref}}{C_{ref}+(1-x'-z)C_a}\right)}\right] \tag{3.2.17}$$

Now that the new voltage between V_{ref} and V_{out} is known, the change in V_{ref} with reference to ground must be found. This is done by noticing the voltage division between the series connection of C_{ref} and $(1-x'-z)C_a$. The change in voltage across C_{ref} is also the change in V_{ref}.

$$\Delta V_{top} = (V_{ref} - V_{out}) - (V'_{ref} - V'_{out}) \tag{3.2.18}$$

$$\Delta V_{ref,z} = \Delta V_{top}\left(\frac{(1-x'-z)C_a}{C_{ref}+(1-x'-z)C_a}\right) \tag{3.2.19}$$

Finally, by putting together the change in V_{ref} associated with the y and z switching

sequences the new V_{ref} can be found.

$$\Delta V_{ref} = \Delta V_{ref,y} + \Delta V_{ref,z} \tag{3.2.20}$$

$$V_{ref,new} = V_{ref} - \Delta V_{ref} \tag{3.2.21}$$

For each sample, N iterations of the y and z switching events occurs, and V_{ref} is decreased after each iteration. While one could use the formula above for analysis, a simpler equation will be derived in the next section.

3.2.3 The Simplified Model

The equations derived above are exact for modelling how the non-ideal switching affects V_{ref}. However, an intuitive understanding of the switching sequence is lost in the complexity of the model. In this section, the model will be simplified to allow for better insight into the relationship between V_{ref}, C_{ref}, C_a, and x, y and z. This model can be simplified using the approximation that C_{ref} is much larger than the input capacitance of the DAC. With this assumption, changes to V_{ref} can be determined by fir assuming V_{ref} is constant ($C_{ref} = \text{inf}$). Then determine how much charge is pulled from V_{ref} after switching. By knowing how much charge, Q, is pulled off of C_{ref}, the new V_{ref} can be calculated.

In this simplified model uses the approximation that C_{ref} is larger than C_a. This can be applied to make calculations in voltage division and changes in V_{ref} simpler. The series capacitance between V_{out} and ground can thus be simplified as shown below. With this approximation, C_{ref} can be ignored when calculating ΔQ.

$$C_{series} = \frac{xC_aC_{ref}}{xC_a + C_{ref}} \approx xC_a \tag{3.2.22}$$

The new analysis begins the same way, by defining x,y and z to signify the groups of capacitance in the charge sharing DAC. x is the fraction of capacitors that are turned on prior to switching.

$$V_{top} = (1-x)V_{ref} \tag{3.2.23}$$

$$V_{bottom} = xV_{ref} \tag{3.2.24}$$

The charge held by a capacitor is its capacitance multiplied by the voltage across it, thus:

$$Q_{top} = x(1-x)C_aV_{ref} \tag{3.2.25}$$

$$Q_{bottom} = (1-x)xC_aV_{ref} \tag{3.2.26}$$

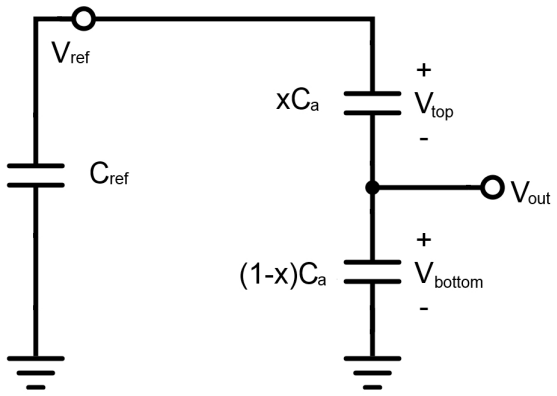


Figure 3.2.6: The DAC capacitor array redrawn to simplify analysis

It is important to note that at this point, prior to switching, the charge across both capacitors are the same.

After the code stored in the SAR is changed, switching occurs instantaneously changing the values of the two capacitances. Like in the previous model, two separate switching sequences will occur per switching cycle. When yC_a is moved down, the new V_{bottom} and V_{top} are:

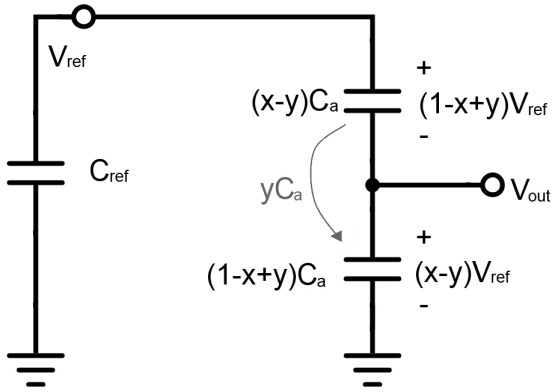


Figure 3.2.7: The y switching sequence for the simplified model

$$V_{top} = (1 - x + y)V_{ref} \tag{3.2.27}$$

$$V_{bottom} = (x - y)V_{ref} \tag{3.2.28}$$

When comparing V_{top} before and after the y switching event, it is evident that the voltage across the top capacitor has changed.

$$\begin{aligned} \Delta V_{top} &= final - initial \\ &= (1 - x + y)V_{ref} - (1 - x)V_{ref} \\ &= yV_{ref} \end{aligned} \tag{3.2.29}$$

Since y must be less than or equal to x, there is a charge flow from the reference into the top capacitor. This charge is given by:

$$\begin{aligned} \Delta Q_{top} &= C_a \Delta V_{top} \\ &= (x-y)C_a \cdot yV_{ref} \\ &= (xy - y^2)C_a V_{ref} \end{aligned} \tag{3.2.30}$$

When looking at the bottom capacitor, there is also a change in voltage. This change in voltage can also imply a change in Q found above. The bottom capacitor can be used to find ΔQ using a similar, yet more involved, calculation seen in Equations 3.2.28 and 3.2.29. This calculation, however, would have the exact same result. Doing both calculations is redundant, thus the simpler calculation shown above is used. Appendix A compares the derivations of ΔQ using the top and then the bottom part of the array, to prove their equivalent result.

The next switching sequence to investigate is when a set of capacitors is moved from bottom to top. The variable z is defined similarly to y to model the value of capacitance being switched, which is outlined in Figure 3.2.8.

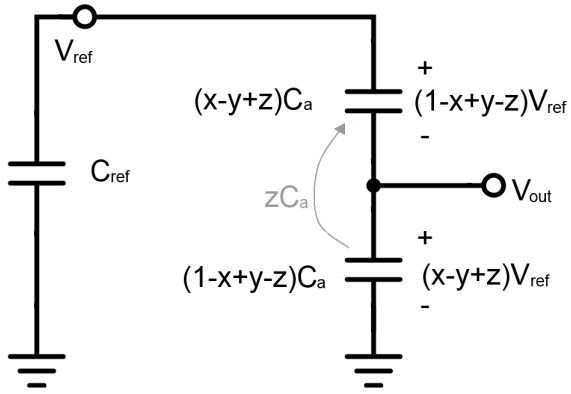


Figure 3.2.8: The z switching sequence for the simplified model

$$V_{top} = (1 - x + y - z)V_{ref} \tag{3.2.31}$$

$$V_{bottom} = (z - y + z)V_{ref} \tag{3.2.32}$$

$$\begin{aligned} \Delta V_{bottom} &= (x - y + z)V_{ref} - (x - y)V_{ref} \\ &= zV_{ref} \end{aligned} \tag{3.2.33}$$

This change in voltage will lead to a net charge flow from the bottom capacitance. Like before, the net charge flow from the top capacitance is not included in the analysis since it would be doubly counted.

$$\begin{aligned} \Delta Q_{bottom} &= C_{bottom} \Delta V_{bottom} \\ &= z(1 - x + y - z)C_a V_{ref} \end{aligned} \tag{3.2.34}$$

Due to the definition of y and z, the sum $(1 - x + y - z)$ will always be positive. Thus, there is a net charge flow from the reference capacitor to the top and bottom capacitances:

$$\begin{aligned} \Delta Q_{total} &= \Delta Q_{top} + \Delta Q_{bottom} \\ &= y(x-y)C_a V_{ref} + z(1-x+y-z)C_a V_{ref} \end{aligned} \tag{3.2.35}$$

Now that how much charge is pulled off the reference capacitor is known, the new V_{ref} seen by the charge sharing DAC can be calculated:

$$\begin{aligned} V_{ref,new} &= V_{ref} - \frac{\Delta Q_{total}}{C_{ref}} \\ &= \left(1 - [y(x-y) + z(1-x+y-z)]\frac{C_a}{C_{ref}}\right) V_{ref} \end{aligned} \tag{3.2.36}$$

By this formula, $V_{ref_{new}} < V_{ref}$. This result is simpler and more intuitive than that seen in Equation 3.2.20.

The largest ΔQ_{total} occurs when the largest capacitor representing the MSB is switched on. This is implies the switching variables will set to $x = 0$, $y = 0$, and $z = 0.5$. Additionally, if the drop in V_{ref} is greater than 1 LSB then the internal DAC will incorrectly output a voltage 1 LSB lower than $\frac{1}{2}V_{FS}$. Equation 3.2.36 can be used to investigate the minimum $\frac{C_a}{C_{ref}}$ ratio required to ensure that the worst case change if V_{ref} is greater than 1 LSB. A ratio of $\frac{C_a}{C_{ref}} \approx 976.5 \times 10^{-6}$ will ensure that this error does not occur.

3.2.4 Validating the Simplified Model

In the simplified model, the calculation to find the new V_{ref} after one switching cycle is far simpler than the more accurate model. The simplicity, however, comes at the cost of additional error. To determine if the error is negligible, the worst case switching sequence will be analysed using both models. The worst case sequence occurs when all capacitors are turned off initially and then a large capacitor is switched on.

$$\begin{aligned} x = y &= 0 \\ z &\neq 0 \\ V_{out} &= 0 \end{aligned} \tag{3.2.37}$$

The algebraic calculations to find the resulting $V_{ref,new}$ using the accurate model is shown in Appendix B. Equation 3.2.37 shows the final result.

$$V_{ref,new} = V_{ref}\left(\frac{1}{1 + z(1-z)\frac{C_a}{C_{ref}}}\right) \tag{3.2.38}$$

Substituting the variables into the simplified model is a much simpler task. The resulting V_{ref} is clearly obtained using Equation 3.2.38.

$$V_{ref,new} = V_{ref}\left(1 - z(1-z)\frac{C_a}{C_{ref}}\right) \tag{3.2.39}$$

The two results are different for each model, though they involve similar terms. To determine the error between the results in Equations 3.2.37 and 3.2.38, certain assumptions can be made. Since $z < 1$ and $C_a < C_{ref}$, it can be concluded that $\left(z(1-z)\frac{C_a}{C_{ref}}\right) \ll 1$. To simplify the analysis, Δ is defined as follows:

$$\Delta = z(1-z)\frac{C_a}{C_{ref}} \tag{3.2.40}$$

This leads to Equations 3.2.37 and 3.2.38 to simplify into:

$$V_{ref,new(exact)} = V_{ref}\left(\frac{1}{1+\Delta}\right) \tag{3.2.41}$$

$$V_{ref,new(simplified)} = V_{ref}\left(1 - \Delta\right) \tag{3.2.42}$$

Next, Equation 3.2.41 can be multiplied by $\frac{1+\Delta}{1+\Delta}$. Then, subtracting this result from Equation 3.2.40, the error is found.

$$Error = \left|\frac{-\Delta^2}{1+\Delta^2}\right| < |\Delta^2| \tag{3.2.43}$$

The Δ can be substituted by $\left(z(1-z)\frac{C_a}{C_{ref}}\right)$. Additionally, $z = \frac{1}{2}$ represents the worst case switching event. Through simplification, the worst case error is bounded as shown below:

$$\Delta^2 \leq \frac{(C_a/C_{ref})^2}{16} \tag{3.2.44}$$

Table 3.2.1 shows how Δ relates to a percent error in V_{ref}. This calculation is shown in Equation 3.2.44.

$$\%Error = \Delta^2 \times 100 \tag{3.2.45}$$

Realistically the change in V_{ref} due to switching must be small enough to ensure at least 12-bit accuracy in the ADC. This is easily achieved when $C_{ref} \gg Ca$. However, C_{ref} decreases, Δ increases towards the same order of magnitude as V_{LSB}. If Δ is in the order of V_{LSB}, then the error associated with using the simplified model is in the order of V_{LSB}^2. In

the case of $\Delta = 1LSB$, a drop of of 1 LSB in V_{ref} shows an error $5.96 \times 10^{-6}\%$ error. Using a V_{ref} value of 1, this implies the error in using the simplified model is $24.4 \times 10^{-3} LSB$. Furthermore, earlier in this section a capacitance ratio $\frac{C_a}{C_{ref}} \approx 976.5 \times 10^{-6}$ was found which ensured the worst case change in V_{ref} to be under 1 LSB. Using this ratio, the error associated with using the simplified model is bounded by 59.6×10^{-9}. Using a V_{ref} of 1, this implies an error of $244 \times 10^{-5} LSB$. This error is sufficiently small enough to justify using the simplified analysis. To express how the error can be considered insignificant, refer to Table 3.2.1.

Table 3.2.1: Error Table

Δ	% Error
0.5	25
0.25	6.25
0.1	1
0.05	0.25
0.01	0.01
$V_{LSB} = \frac{1}{2^{12}}$	5.96×10^{-6}

The simplified model is a very good approximation of the behaviour of the ADC due to a non-ideal reference capacitance. This simplified model will be the model used for simulation and analysis.

The analysis done in this chapter so far has assumed that the voltage reference circuit is represented by a large capacitor labeled C_{ref}.

3.3 Analysis of The Voltage Reference Circuit

The linearity of the SAR-ADC is highly dependent on the performance of the voltage reference. The voltage reference circuit used in for this thesis, and for many other SAR-ADC networks, is the bandgap reference circuit. The issue with this circuit is that it has poor performance when it is loaded with a high frequency varying load. When the load varies, perturbations are seen in the reference voltage. To solve this issue a bypass capacitor, or decoupling capacitor, is connected in parallel with the load which reduce perturbations in the reference voltage. In this section, the voltage reference and bypass capacitor are analysed. This is done from the perspective of the reference voltage pin of the ADC looking into the output of the voltage reference and bypass capacitor circuit.

The bandgap reference circuit is a complex circuit which provides a temperature independent voltage while consuming a small amount of power [9]. This circuit will not be fully

analysed for this thesis, however Figure 3.3.1 shows the functional block diagram of the reference used in Chapter 4.

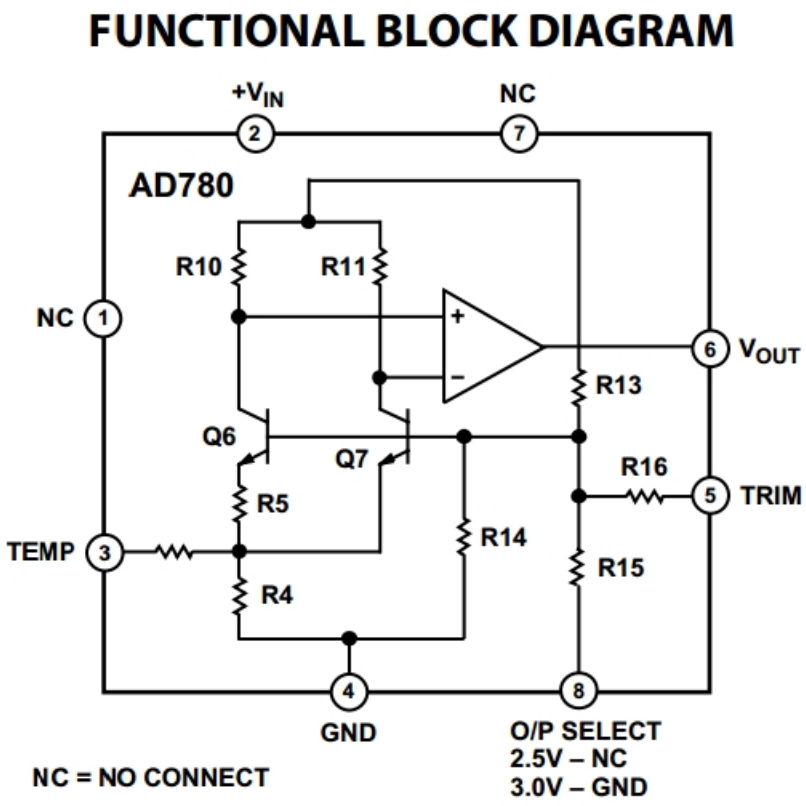


Figure 3.3.1: Functional Block Diagram For the AD780 Bandgap Voltage Reference Circuit [12]

For analysis purposes, the bandgap reference circuit can be replaced by an equivalent circuit. This equivalent circuit will have an ideal voltage source, and a frequency dependent impedance. The output of a reference circuit is buffered by an operational amplifier, which sets the reference circuit's output impedance. Typically the output impedance nominally 10Ω at a few hundred kHz. The impedance then rises at 6 dB/octave [9]. This impedance can be modelled by a resistor and inductor connected in series. Figure 3.3.2 shows the typical response of the output impedance, and the equivalent circuit for the voltage reference.

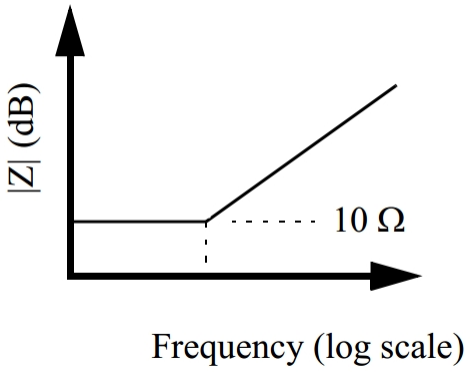


Figure 3.3.2: Typical Output Impedance Response for an Output Buffered Reference [9]

When looking into the internal charge sharing DAC, it is clear that it is a transient load that changes at a very high frequency. The SAR-ADC used in this thesis is a 12 bit ADC that operates at 3 mega-samples per second. For each sample, the internal DAC switches the capacitance values a minimum of 12 times. This implies that the frequency at which the load is changing is atleast $36MHz$. This frequency is much greater than a few hundred kHz, by two orders of magnitude. This implies that the output impedance is also two orders of magnitude larger, or within the $k\Omega$ range.

To reduce the output impedance of the reference circuit, a bypass capacitor is placed at the output. The impedance of this capacitor is defined by Equation 3.3.1. A typical value of the bypass capacitor is $10\mu F$. This implies that at the same frequency, the impedance of the bypass capacitor is approximately $442\mu\Omega$, which is significantly smaller than that of the voltage reference itself. Even at $10nF$, the lowest tested reference capacitance, the impedance of the bypass capacitor is orders of magnitude smaller than that of the output impedance of the voltage reference circuit. Since the bypass capacitor is placed in parallel to the output resistance of the reference circuit, the total output resistance is practically equivalent to the bypass capacitor itself.

$$Z_c = \frac{1}{j2\pi C_{bypass}} \tag{3.3.1}$$

In its steady state, the bypass capacitor is charged to V_{ref} by the reference circuit. Correspondingly, The output voltage of the total circuit containing the reference and the bypass capacitor is V_{ref}. Since charge is pulled from the voltage reference every time the capacitive array switches, it can be looked at as a high frequency varying current. At this high frequency, the impedance of the bypass capacitor is much smaller than the output resistance of the voltage reference circuit. This is because the majority of the charge, if not all of the

charge, will be pulled off the reference capacitor as it provides the low impedance path. Consequently, the voltage reference circuit can be considered to be an open circuit for analysis purposes. Furthermore, the bypass capacitor and voltage reference circuit will be simplified into a single capacitor, known as the reference capacitor, C_{ref}, which is fully charged to V_{ref} at the beginning of a switching sequence.

3.4 Modelling the Non-Ideal Behaviour in Matlab

This chapter began with the implementation of an ideal successive approximation ADC in Matlab model. This model simplified the voltage reference and bypass capacitor into a single capacitor charged to V_{ref}, which is connected to a binary weighted array of switched capacitors. These switched capacitors together form the internal charge sharing DAC of the SAR-ADC. By investigating the switching behaviour of the charge sharing DAC, non-ideal behaviour of the reference voltage was determined. After the instantaneous switching of ideal switches rearranged the capacitance array, some charge was lost to ground and some was pulled from the reference capacitance. By pulling charge from the reference capacitance, the voltage held was decreased. This reduction in the reference voltage will lead to the output of the DAC to be lower than the ideal value. Additionally, $Vref$ will change each time the SAR is adjusted. This means that the error associated with this non-ideal behaviour is code dependent. This relationship is evident since the new V_{ref} value after switching is a function of x, y, and z. Below is the code which includes all the non-ideal modelling analysed in this chapter, which was added to the ideal successive approximation algorithm.

```
    %initialize x, y and z
    y=0;
    x=0;
        for i=1:12
            %update z to pull-up the next capacitor in sequence
            z = 1/2^i;

            %Vref new after charge sharing between Cr and Capacitive array
            Vref = (1-(y*(x-y)+z*(1-x+y-z))*Cap/Cr)*Vref;

            Vdac = (x-y+z)*Vref;

            %update x for next iteration
            x = x-y+z;
            if vin(r,c) < Vdac
                b(i) = 0;
                y = z;  % capacitor is returned back down
            else
                b(i)=1;
                y=0;    % capacitor remains top
            end

        end
```

Figure 3.4.1: Matlab Code for a Non-Ideal Successive Approximation ADC

This model can be used to generate a non-ideal FFT shown in Figure 3.4.2. In this FFT, distinct harmonics are visible, and the noise floor contains distortion spurs as well as quantization noise.

Previously in this chapter, calculations were made to approximate the the minimum $\frac{C_a}{C_{ref}}$. However, the validity and accuracy of this finding cannot be justified until it is proven to predict real-world applications. In order to properly identify what ratio is needed, more data is needed. This data can be acquired by through simulations based on the analysis done. However, in order to identify a realistic starting point and practical values for the required capacitance values, measurements from a real SAR-ADC are needed.

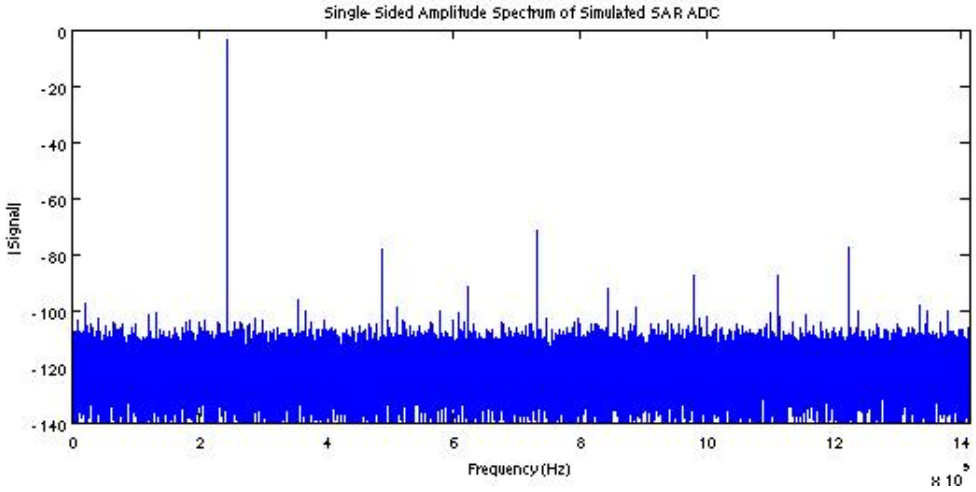


Figure 3.4.2: Sample FFT Response from a Simulated Non-Ideal ADC

Chapter 4

Measurements

During the research process, testing on a successive approximation analog to digital converter (SAR-ADC) was done in parallel with the circuit analysis done in Chapter 3. The analysis was presented first since it provides valuable context to understand and interpret the measured results. This chapter will present methodology and the outcomes of lab measurements used to identify how the bypass capacitor relates to the distortion seen at the output of the SAR-ADC. To begin this chapter, a quick summary of the equipment used to take measurements will be provided.

4.1 Test Setup and Equipment

The experiment has been set up as follows. The signal generator is connected to the evaluation board through a low pass filter. The evaluation board is controlled by the evaluation controller board. The controller board provides the evaluation board with a voltage reference and clock signal, and measures the output of the AD7276 chip. The controller board is connected to a PC, which is loaded with software that interprets the digital output. This software is an application built with NI LabView. It is able to window a set of samples taken from the evaluation board and output a FFT plot. The software also displays all necessary measurements. Figure 4.1.1 shows a block diagram of how the apparatus is assembled.

Figure 4.1.1: Block Diagram of Equipment Used For Measurements and Interconnections

4.1.1 The Successive Approximation ADC

The SAR-ADC used during measurements is the AD7276 by Analog Devices. It has a resolution of 12 bits, and a maximum throughput rate of 3 MSPS [7]. The AD7276 is a 6-pin integrated circuit. Two pins are dedicated to the power supply (VDD) and ground (GND). VDD represents the full-scale voltage, and is also used as the reference voltage for the SAR-ADC's internal DAC. The third input is used for the input signal (Vin), which is an analog signal from 0 to VDD. Two inputs are dedicated for the SAR-ADC's timing controls, which are the system clock (SCLK) and the chip select signal (CS). Finally, the AD7276 has one pin dedicated for the digital output (SDATA) [7]. The pin diagram for the AD7276 can be seen in Figure 4.1.2. The relevant dynamic performance and timing specifications for the AD7276 can be found in Appendix C [7].

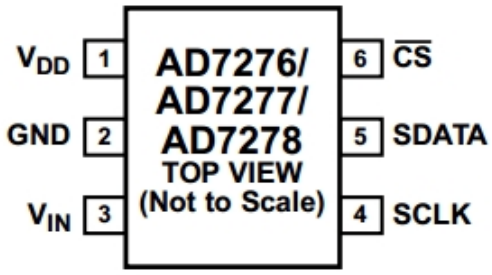


Figure 4.1.2: Pin Diagram For the AD7276 Successive Approximation ADC [7]

4.1.2 The Evaluation Board

The evaluation board is used to evaluate all the features of the AD7276 SAR-ADC. The evaluation board is the EVAL-AD7276SDZ by Analog Devices. It interfaces the AD7276 IC by providing connections to the VDD, GND, Vin, CS, SCLK and SDATA inputs of the chip. The interface is designed to provide low-noise, low-distortion, and stable measuring environment for the SAR-ADC [13]. The evaluation board was designed to allow for either user provided controls or to use a controller board to control the AD7276. The evaluation board is used since it is well suited for the task of taking sufficient measurements for the purposes of this thesis. Refer to Appendix D for further details on the EVAL-AD7276SDZ.

4.1.3 The Controller board

A controller board is used to interface the EVAL-AD7276SDZ to a PC for data collection. The controller board used is the EVAL-SDP-CB1Z by Analog Devices. It houses a 600 MHz Blackfin processor, 32 Mb flash memory and SDRAM memory [14]. The controller board

connects directly to the evaluation board via a 120 pin connector, and to the PC via USB. In addition to interfacing the evaluation board with the PC, the controller board provides the evaluation board with VDD, GND, CS and SCLK. This simplifies the process of evaluating the AD7276 by simply requiring the tester to provide an analog input, Vin, to begin testing. The controller board then reads the SDATA signal from the AD7276, then feeds the data to the PC. Software is then used to interpret the data and output relevant information regarding the signal quality [14]. Refer to Appendix E for further details on the EVAL-SDP-CB1Z.

4.1.4 The Signal Generator

The input signals used for measurements were generated by the Rohde & Shwarz SMA100A Signal Generator. The SMA100A provides very low phase noise and nonharmonics [15]. However, this signal generator generates low power harmonics. Though this signal generator can generate signals of a wide range of frequencies, it was found that the power of the harmonics was minimized at lower frequencies below $400kHz$. Thus, input frequencies within the range of $200kHz$ to $350kHz$ were used. Additionally, a low pass filter was required to further attenuate these harmonics to reduce interference while measuring the distortion generated by the AD7276 itself. Refer to Appendix F for further details on the R&S SMA100A Signal Generator.

4.1.5 The Filter

A low pass filter was used to filter noise and distortion coming from the signal generator. The low pass filter was designed by KR Electronics. The filtering response can be seen in Figure 4.1.3 below. This filter was selected because it provided a sharp roll-off after a low frequency cut-off of $350kHz$ [16]. The low pass filter connects to the signal generator and evaluation board via SMA coaxial cables. Refer to Appendix G for further details of KR 2827.

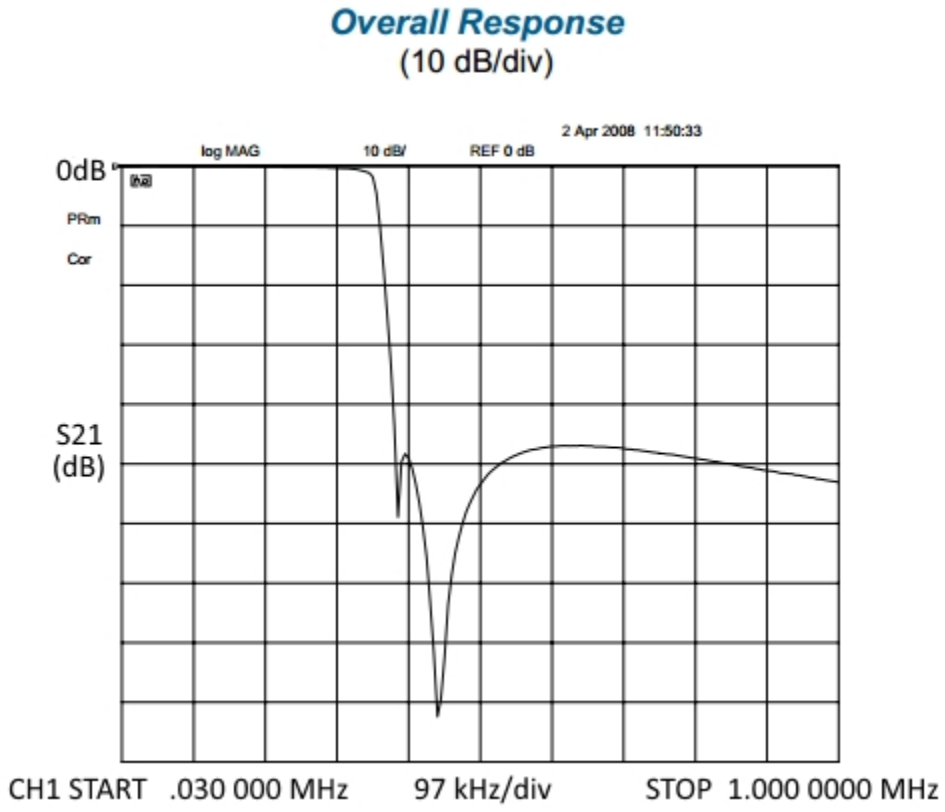


Figure 4.1.3: Overall Frequency Response of the KR 2827 Low-pass Filter [16]

4.2 Typical Results and Experimental Procedure

In this section, typical measurement results from the AD7276 SAR-ADC evaluation board will be presented. Figure 4.2.1 and Figure 4.2.2 show the outputs recorded from a single measurement. Figure 4.2.1 shows the most relevant measurement as it pertains to the dynamic testing of the ADC. The figure shows the FFT representation of the measured data. Additionally under Spectrum Analysis, information of the signal power, harmonics and dynamic specifications are shown. Figure 4.2.2 shows a complete summary of the measurements taken. Firstly the waveform is shown, which at first looks like a white rectangle. However, it is a compressed sinusoidal signal. It is important to note that the signal does not cover the full-scale voltage range. This can also be seen from the histogram, as it does not cover the full range of output codes. Under Data Capture Summary, the Signal to Noise Ratio (SNR), Total Harmonic Distortion (THD), Signal to Noise and Distortion Ratio (SNDR), and Dynamic Range (SFDR) are calculated and displayed. It should be noted that the software labels SNDR as S/N+D, and that they are equivalent in meaning.

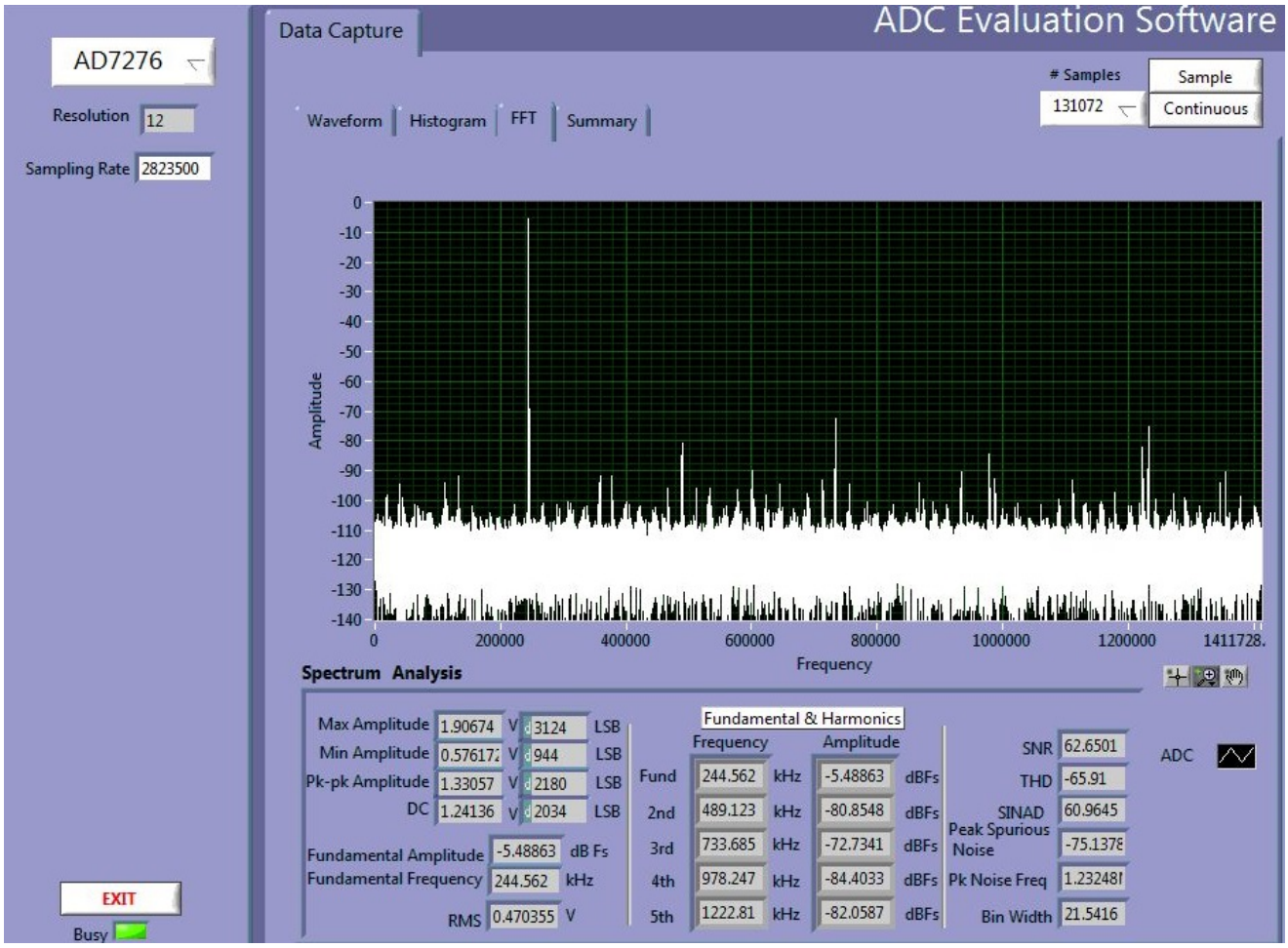


Figure 4.2.1: Sample Measurement Output Screen 1

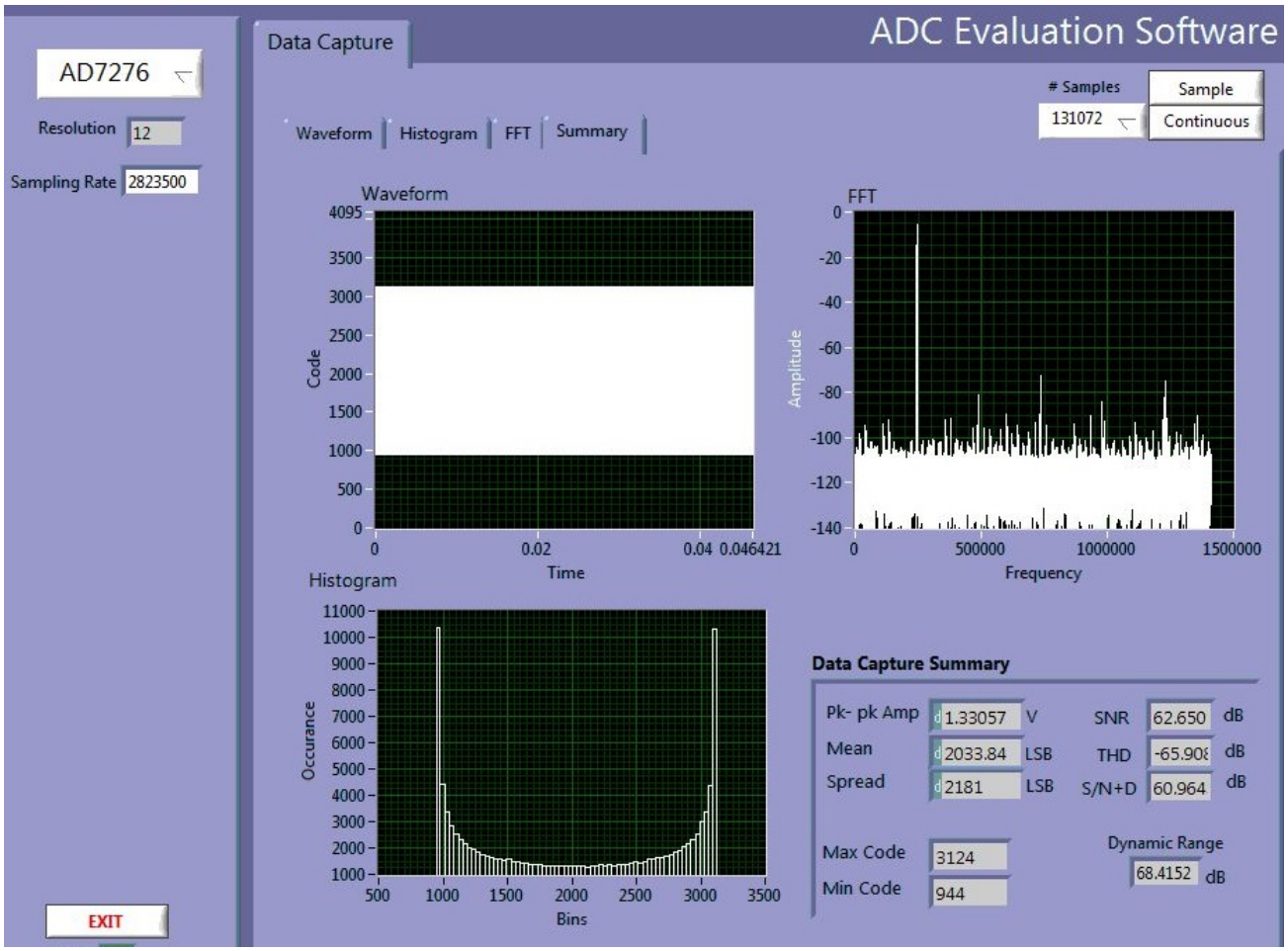


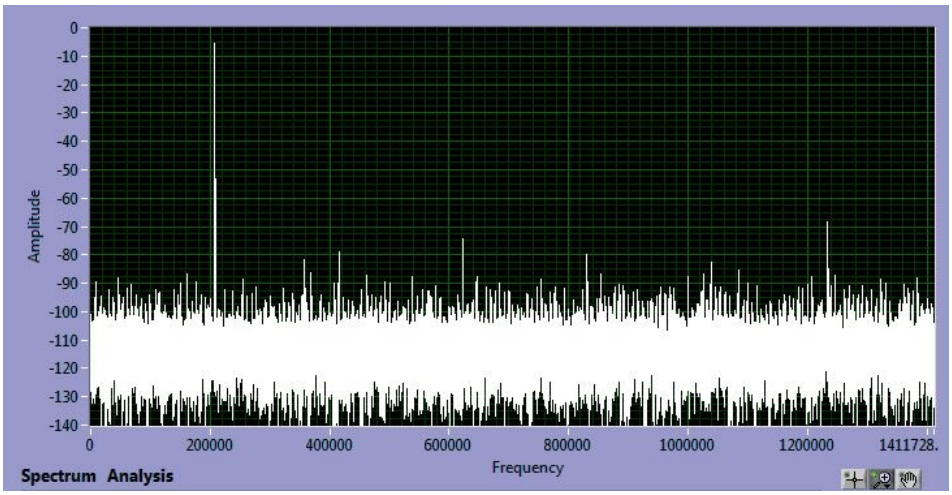
Figure 4.2.2: Sample Measurement Output Screen 2

The controller board is used to control the timing of the evaluation board and the AD7276 SAR-ADC. For all the measurements taken in the experiment, a sampling rate of 2823500 samples per second was used. Though the AD7276 is rated to operate at 3 Mega samples per second, operating at this speed resulted in errors with the software. Furthermore, 131072 (2^{17}) samples were taken per measurement. This allowed for sufficient resolution in the reconstructed signal, and accuracy in the dynamic measurements.

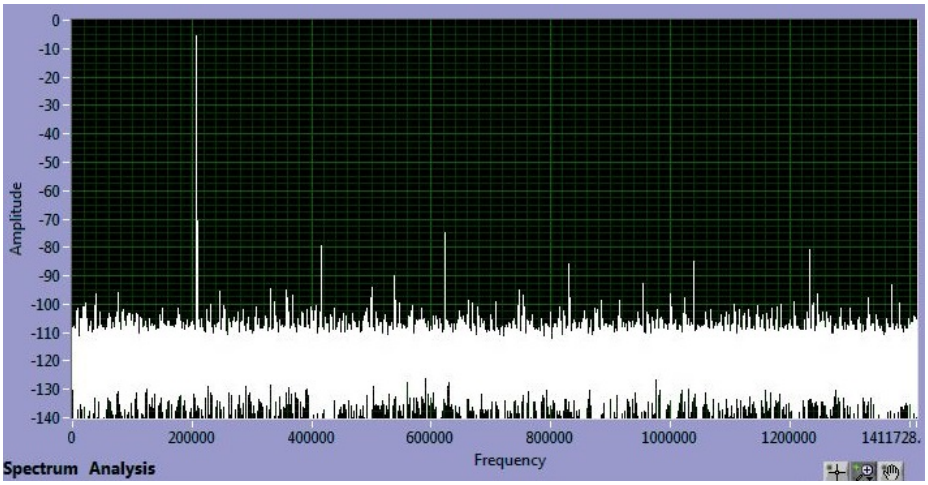
On the evaluation board, where the AD7276 SAR-ADC is installed, is the bypass capacitor. In Chapter 3 it was shown that the bypass capacitor value plays a significant role in the linearity of the ADC. This bypass capacitor along with the voltage reference circuit are represented by an equivalent circuit of a single capacitor referred to as the reference capacitor, C_{ref}. In this experiment, the bypass capacitor will be replaced with a variety of different sized capacitors in order to characterize how the ADC's distortion relates to C_{ref}.

Measurements seen in Figures 4.2.1 and 4.2.2 were taken each time the reference capacitor was changed. Figure 4.2.3 shows three FFT plots from a small reference capacitor of $10nF$,

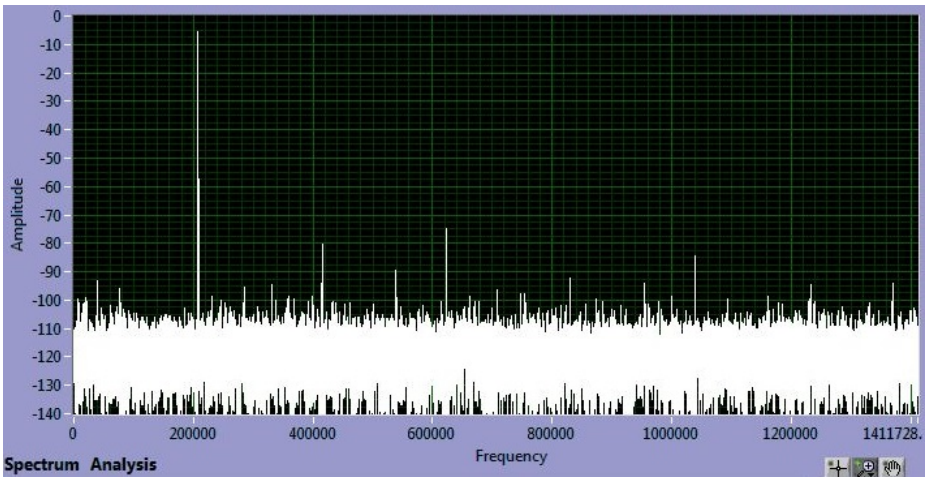
an in-between sized capacitor of $0.47\mu F$, and a large capacitor of $100\mu F$. The purpose of this figure is to show how the signal quality changes in the FFT as the reference capacitor is changed. When looking at how the FFT is changing between the three plots, it is clear that the signal quality improves as the reference capacitor increases in size. The noise floors rest between approximately $-100dB$ and $-110dB$ in all three cases. At lower reference capacitance, spurs caused by distortion are apparent throughout the spectrum. The most prominent spurs are the first four harmonics. As reference capacitance increases as shown in Figure 4.2.3b, the smaller spurs begin to decrease in power. This causes the noise floor to decrease slightly since distortion terms beyond the first four harmonics are considered as noise. Also, the reduction in these spurs reveals that the first four harmonics remain distinct and unchanged. At $100\mu F$, or large reference capacitance, the spurs are much smaller such that the noise floor looks like it has decreased closer to $-110dB$. The second, third and fourth harmonic look unchanged, while all other distortion terms are attenuated. This is not close to an ideal response as shown in Figure 3.1.2 of Chapter 3. However, Figure 4.2.3c represents the best case response for the AD7276 while within the environment of the evaluation board.



(a) $10nF$ Reference Capacitor



(b) $0.47\mu F$ Reference Capacitor



(c) $100\mu F$ Reference Capacitor

Figure 4.2.3: Three Sample Measured FFT Plots

4.2.1 Unexpected Difficulties of Experimentation

Once the equipment had been set-up, the off-chip reference capacitors must be varied and the ADC's performance measured. Firstly, the capacitance must be identified on the evaluation board itself. Going through the schematic, capacitors C33 and C34 connected in parallel make up C_{ref} as defined in the analysis. The reason why these two capacitors are in parallel is that C33 is a large electrolytic capacitor, while C34 is a smaller ceramic capacitor. C33 provides a large capacitance, at a lower cost compared to a dielectric capacitor of the same high capacitance. It is able to hold V_{ref} high, however because of the intrinsic properties of electrolytic capacitors, it has large equivalent series resistance (ESR) and inductance (ESL). This implies that the electrolytic capacitor is not suitable for decoupling purposes by itself. The smaller ceramic capacitor has a significantly lower ESR and ESL. However, the smaller ceramic capacitor cannot hold enough charge required to maintain the reference voltage. Thus by putting them in parallel, the design allows the large capacitor to function as a large capacitance bank for long term use, and the small capacitor provides a small amount of capacitance quickly for instantaneous switching.

The costs associated with using large ceramic capacitors are small when they are not considered for mass production. Thus both C33 and C34 will be replaced by a single ceramic capacitor. This larger ceramic capacitor, C_{ref} can hold the required charge to hold V_{ref} without the instantaneous drops in voltage due to high ESR. C_{ref} will be varied and the performance of the ADC will be measured using the previously described apparatus. The capacitors used in the experiment are shown in in Table 4.2.1. These capacitors are all the same package size. They are manually soldered on the C33 pads. For each capacitor used, a set of measurement results were recorded through the controller board's software.

Table 4.2.1: Capacitors Used to Vary Reference Capacitance

$10nF$	$22nF$	$47nF$
$0.1\mu F$	$0.22\mu F$	$0.47\mu F$
$1\mu F$	$2.2\mu F$	$4.7\mu F$
$10\mu F$	$22\mu F$	$47\mu F$
$100\mu F$	Open Circuit	

In addition to taking measurements for each of the reference capacitors, four different input frequencies were used. This was done to determine if there existed a relationship between input frequency and the ADC's output distortion. The four frequencies used in the experiment are shown in Table 4.2.2. They are approximated to $207kHz$, $244kHz$, $285kHz$, and $327kHz$. These frequencies were chosen since the distortion from the signal generator

was minimized at frequencies less than approximately $400kHz$. This was found by scanning frequencies and measuring the distortion via the AD7276 evaluation board. At this point, the low pass filter was chosen to further improve the distortion, with a cut-off frequency close to the input frequencies chosen. The goal was to choose frequencies approximately $40kHz$ apart. Additionally the frequencies were chosen according to Equation 4.2.1, such that the frequency fits in a FFT bin and does not spread across the spectrum. F_{in} is the input frequency, N is a prime number, L is the number of samples, and F_s is the sampling rate.

$$F_{in} = \frac{N}{L} F_s \tag{4.2.1}$$

Table 4.2.2: Table of Input Frequencies, Input and Output Ranges using a $9dBm$ Input

Frequency (Hz)	Amplitude (V_{pk-pk})	Output Spread (codes)
207725.605	1.356	2223
244561.733	1.327	2175
284973.766	1.312	2151
326850.628	1.264	2072

Two amplitudes were also used to investigate if the input signal's amplitude relates to distortion seen at the ADC's output. Only two signal powers were used, $9dBm$ and $11dBm$. This equates to approximately $1.35V_{pk-pk}$ and $1.7V_{pk-pk}$ at the input of the ADC, and a spread of 2250 codes and 2835 codes. These amplitudes were chosen because as the amplitude increased, distortion from the signal generator increased as well. For this reason, a full-scale input could not be used. Additionally if the signal power is too low, the output spread would also decrease. If the spread is too low then conclusions about the distortion may be deemed inconclusive.

An unintended result of varying frequencies is that the amplitude measured at the input pin of the AD7276 board changed. The variation in amplitude may be due to internal filtering that exists within the signal path between the coaxial input and the input of the AD7276 chip. Table 4.2.2 shows the corresponding amplitude for each frequency used. Though unintended, one benefit of this is that the relationship between amplitude and distortion can be seen without varying the amplitude on the signal generator itself. As previously discussed, the output distortion of the signal generator was proportional to the signal's amplitude. Thus, by keeping the amplitude set on the signal generator constant, the distortion due to the signal generator also remained constant.

In the first part of the next section, only one data generated using the $9dBm$ input will be considered. The four frequencies and the 14 reference capacitors create 56 points. Using these 56 measurements, characteristic plots for SNDR, SNR, THD, and SFDR are created comparing the dynamic measurements to reference capacitance.

4.3 SNR, SNDR, THD, and SFDR vs Reference Capacitance

This section shows data showing the relation between different dynamic specifications and a varying bypass capacitor, or reference capacitance. These plots all show a similar indication of distortion growing as the reference capacitance decreases. These results are repeatable, and have been tested using several different boards.

The Measured SNDR Characteristic

The first plot to be investigated is shown in Figure 4.3.1, which shows the relationship between reference capacitance and SNDR. The SNDR represents the ratio of signal power to the combined total noise and distortion power. There are four separate curves in this figure, one for each of the input frequencies used. The first characteristic of the plot that should be noted is the constant separation between these four curves. This separation can be explained by the decrease in signal power as shown in Table 4.2.2. Additionally, it could imply a constant variation due to the change in input frequencies.

The general shape of the curve shows an S-shaped characteristic. This shape will be seen again in future plots. The noise and distortion are saturated at high capacitance and also at low reference capacitance. An exponential increase in distortion between $10nF$ and $1\mu F$ connects these saturation levels. From the plot, it can be seen that increasing the reference capacitance greater than approximately $1\mu F$ will not result in any improvement to the SNDR.

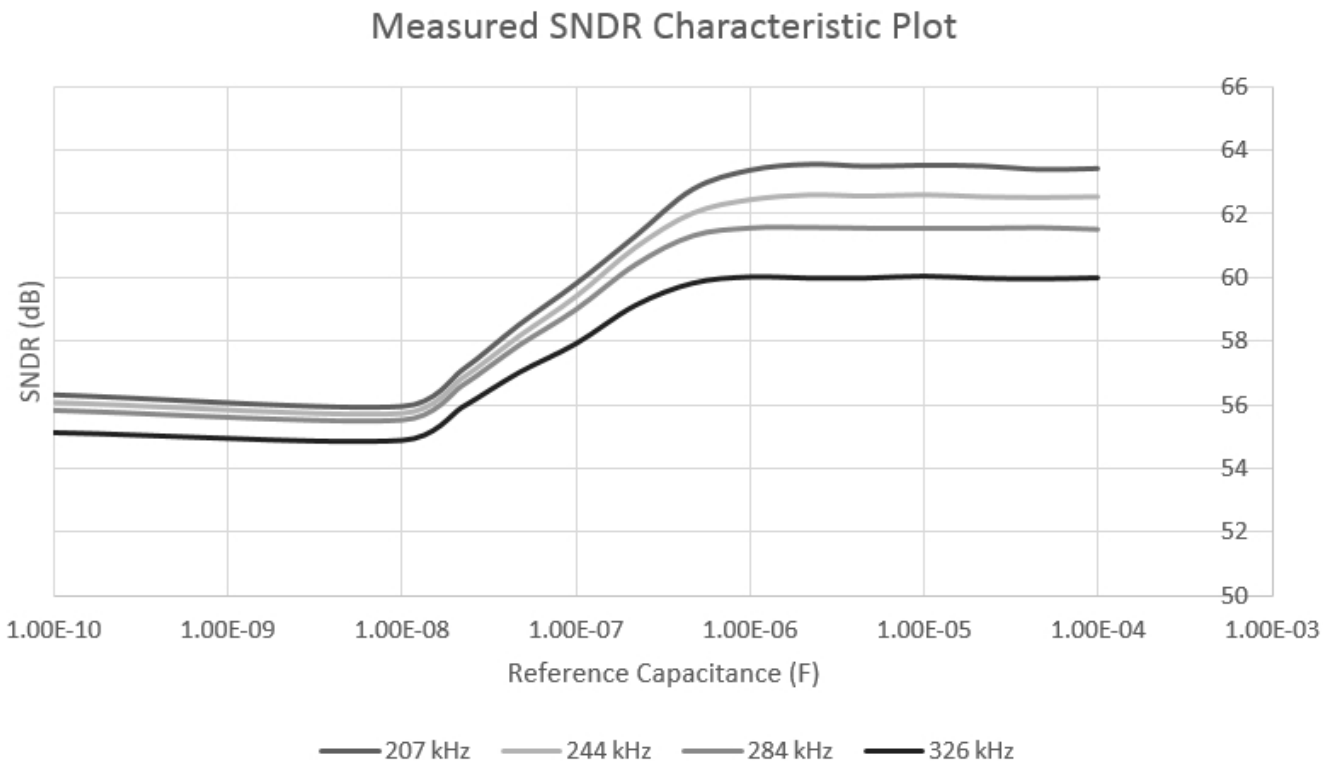


Figure 4.3.1: Measured SNDR versus Reference Capacitance

The Measured SNR Characteristic

The SNR plot ignores the first five harmonics and compares all other terms to the signal. This includes all the noise power, but also distortion terms beyond the sixth harmonic, which are aliased back into the spectrum. When looking at Figure 4.3.2, the SNR shows the same S characteristic curve, similar to SNDR plot. The noise power and smaller harmonics are saturated at higher and lower reference capacitance, and rise exponentially in between these two levels. SNR shows significantly less separation between the four curves. This implies that the first five harmonics show a dependence on the signal amplitude and/or frequency. However, the noise and distortion terms included in the SNR calculation do not vary significantly with the signal's amplitude or frequency. This can be seen further in Figure 4.3.3, which shows the THD versus reference capacitance.

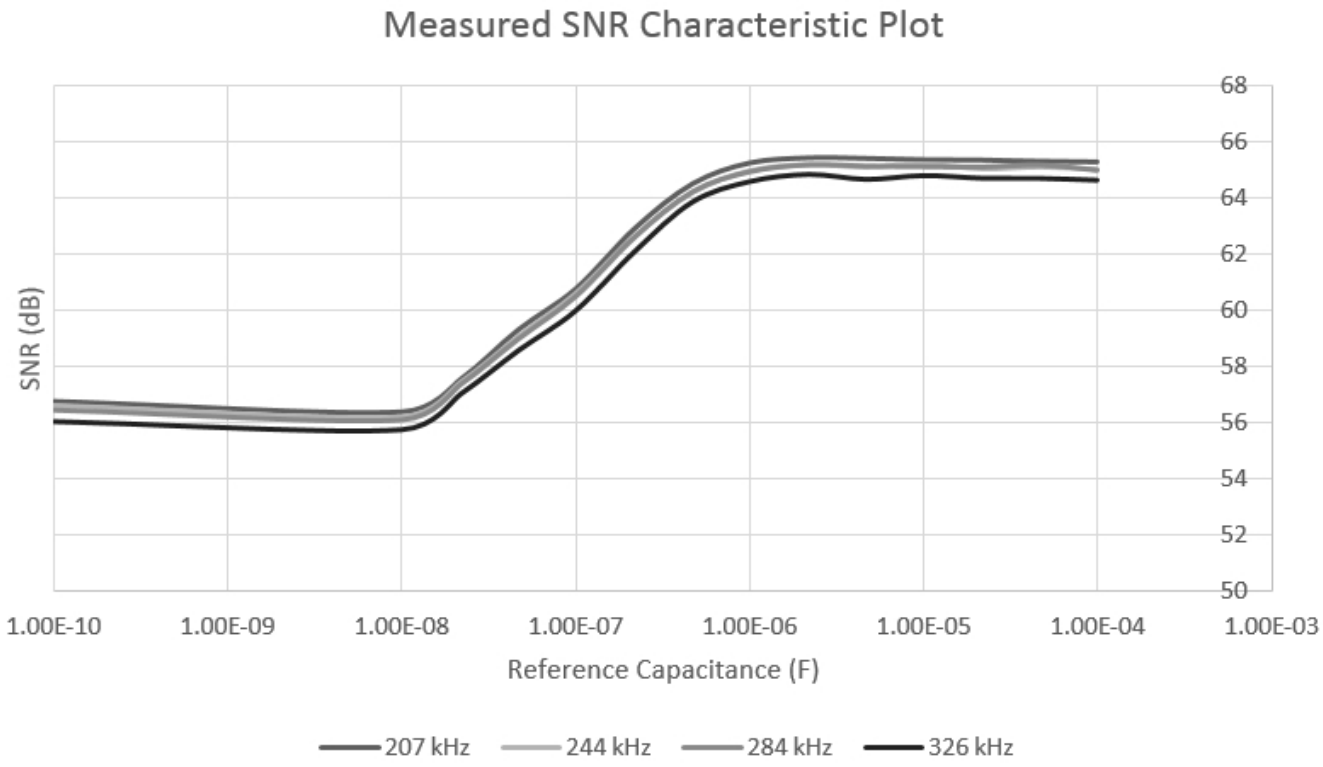


Figure 4.3.2: Measured SNR versus Reference Capacitance

The Measured THD Characteristic

The THD calculation includes the first 5 harmonics, as all other distortion terms are grouped together as noise. The THD is relatively constant as reference capacitance changes. This explains why the SNDR shows a constant separation between the four curves while the SNR plot does not. Additionally, this result shows that the first 5 harmonics are relatively independent of the reference capacitance. At high reference capacitance, the distortion curves are separated by approximately 20 dB each. Approximately every $40kHz$ increase in input frequency results in a $20dB$ increase in THD. Alternatively, this could also imply that as amplitude decreases the distortion increases. At this point, it is uncertain whether the relationship is dependent on frequency, amplitude, or both.

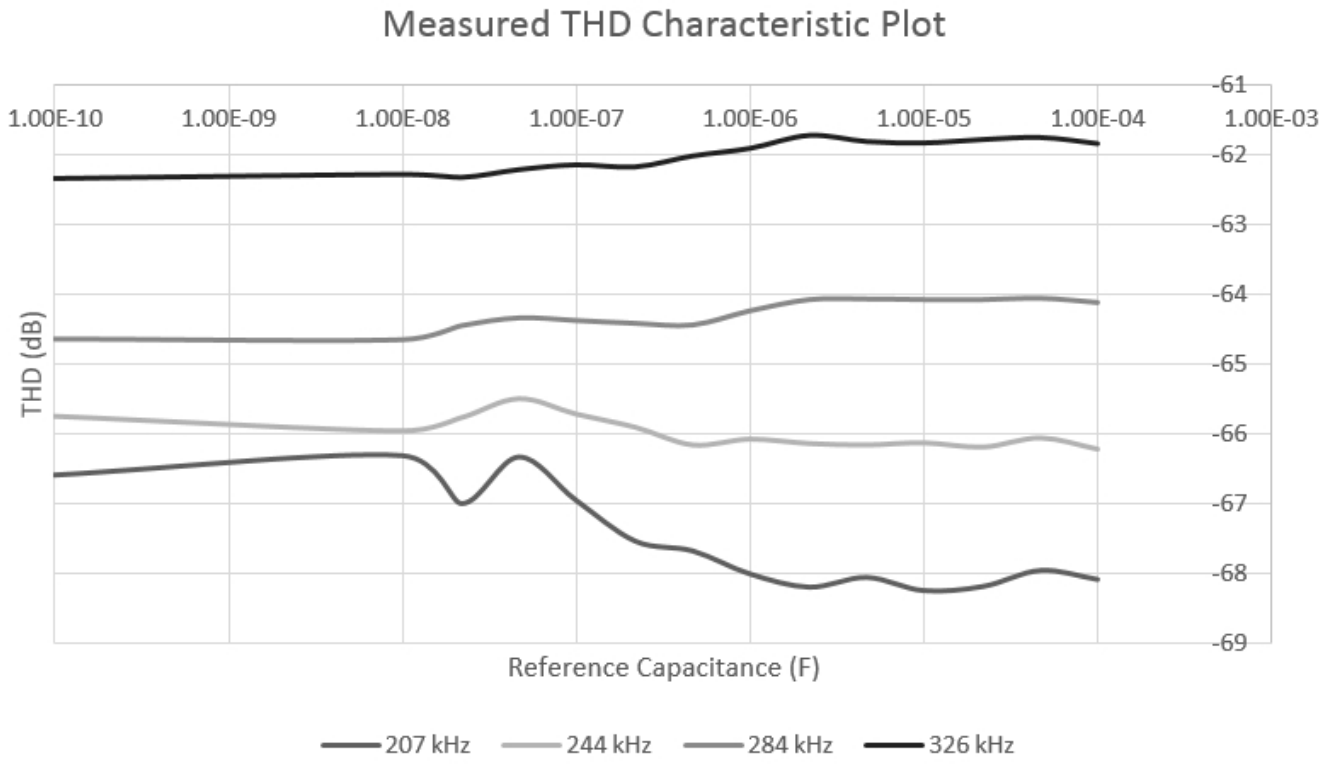


Figure 4.3.3: Measured THD versus Reference Capacitance

The Measured SFDR Characteristic

Figure 4.3.4 shows that the SFDR characteristic curves, across all four frequencies, are approximately the same. Thus the response is independent of frequency and amplitude. The relationship between the largest spur and the signal power is very dependent on reference capacitance, as it has the same characteristic S-shaped curve seen in the SNDR and SNR plots. It is expected that the largest spurs will be identified as a harmonic distortion term. However, since the THD relationship is relatively constant with varying reference capacitance, the S-shaped relationship between SFDR and reference capacitance cannot be explained. When looking at Figure 4.2.3, it can be seen that an additional spur near $1.23MHz$ exists, which is larger than the third harmonic. Because it is the largest distortion spur, it limits in the SFDR. This spur decreases as reference capacitance increases, and is not one of the harmonics included in the THD calculation. This is why the SFDR curve shows the S-shaped characteristic while the THD curve does not.

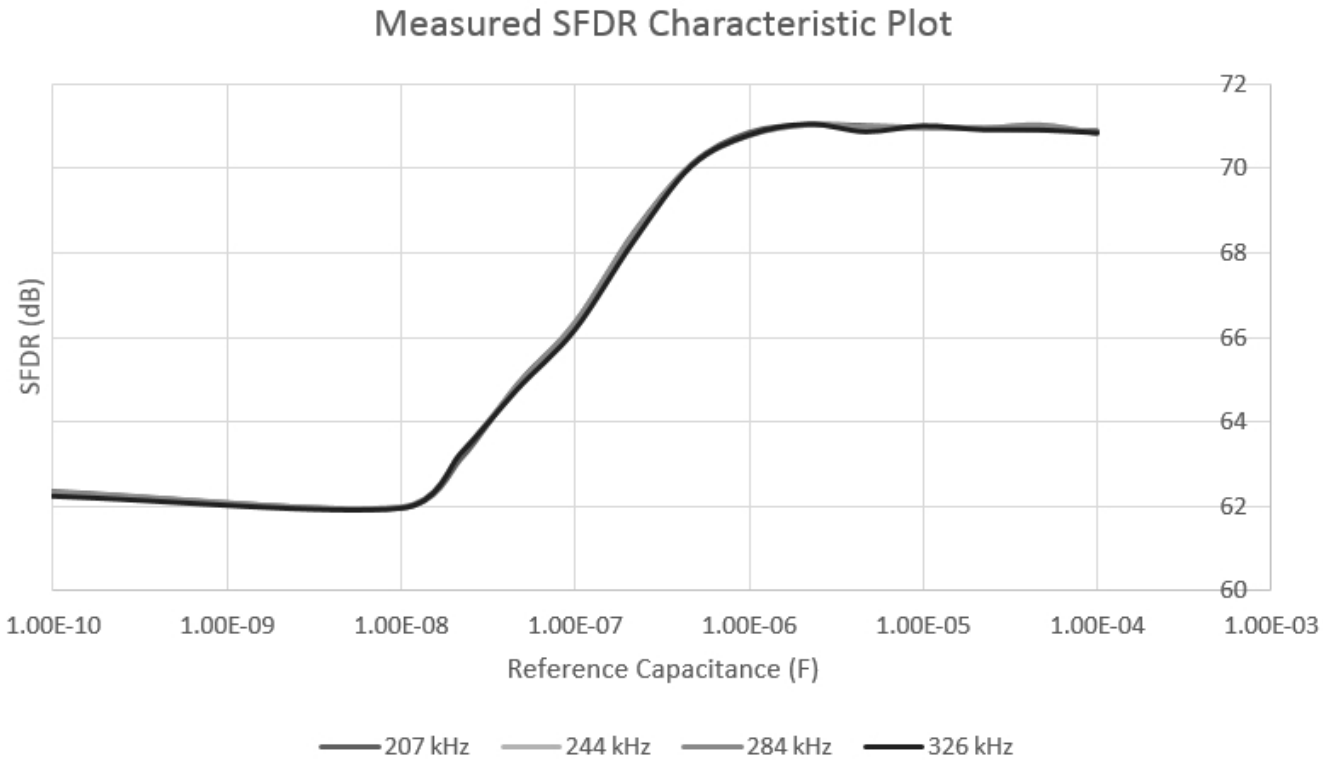


Figure 4.3.4: Measured SFDR versus Reference Capacitance

4.3.1 Comparing Different Input Voltage Levels

At the beginning of this section, it was discussed that two amplitudes were tested; one being $9dBm$ and the other $11dBm$. In this part of the section we will look at the same SNDR, SNR, THD, and SFDR plots comparing the measurements of the two input amplitudes. Figure 4.3.5 shows the relationship between SNDR and reference capacitance. SNDR between both measurements are approximately the same. The trial with lower amplitude shows slightly better SNDR, especially between $10nf$ and $1\mu F$.

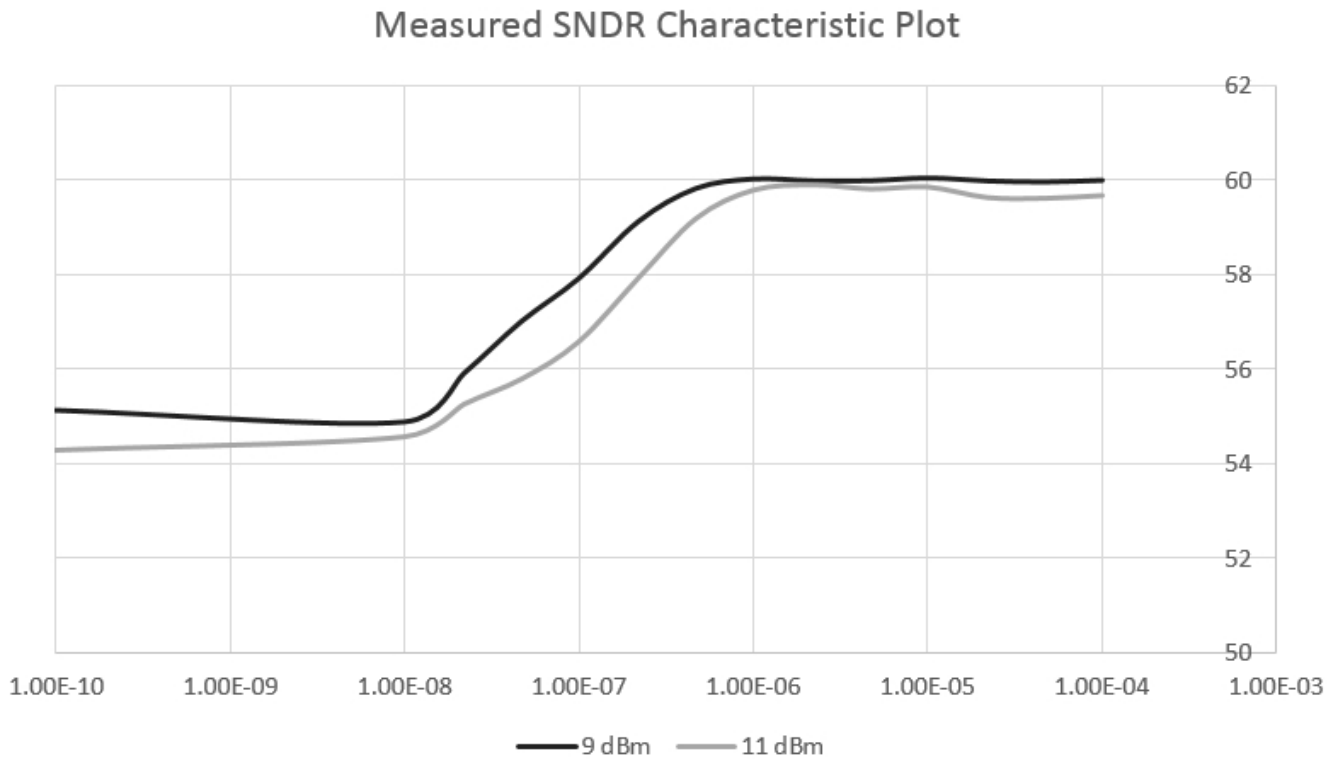


Figure 4.3.5: Measured SNDR versus Reference Capacitance for 9dBM and 11dBm Signals

Figure 4.3.6 shows the SNR characteristic curve. This curve shows that the larger amplitude has a better SNR ratio. This is because the noise floor remains relatively constant between the two measurement trials, thus higher signal power would improve the SNR. At capacitances under $1\mu F$, the distortion terms beyond the fifth harmonic begin to grow exponentially. Since they counted as noise terms, the SNR characteristic shows the expected S-shape. Since the harmonics are proportional to signal power, the SNR of the two curves begin to converge at lower capacitances.

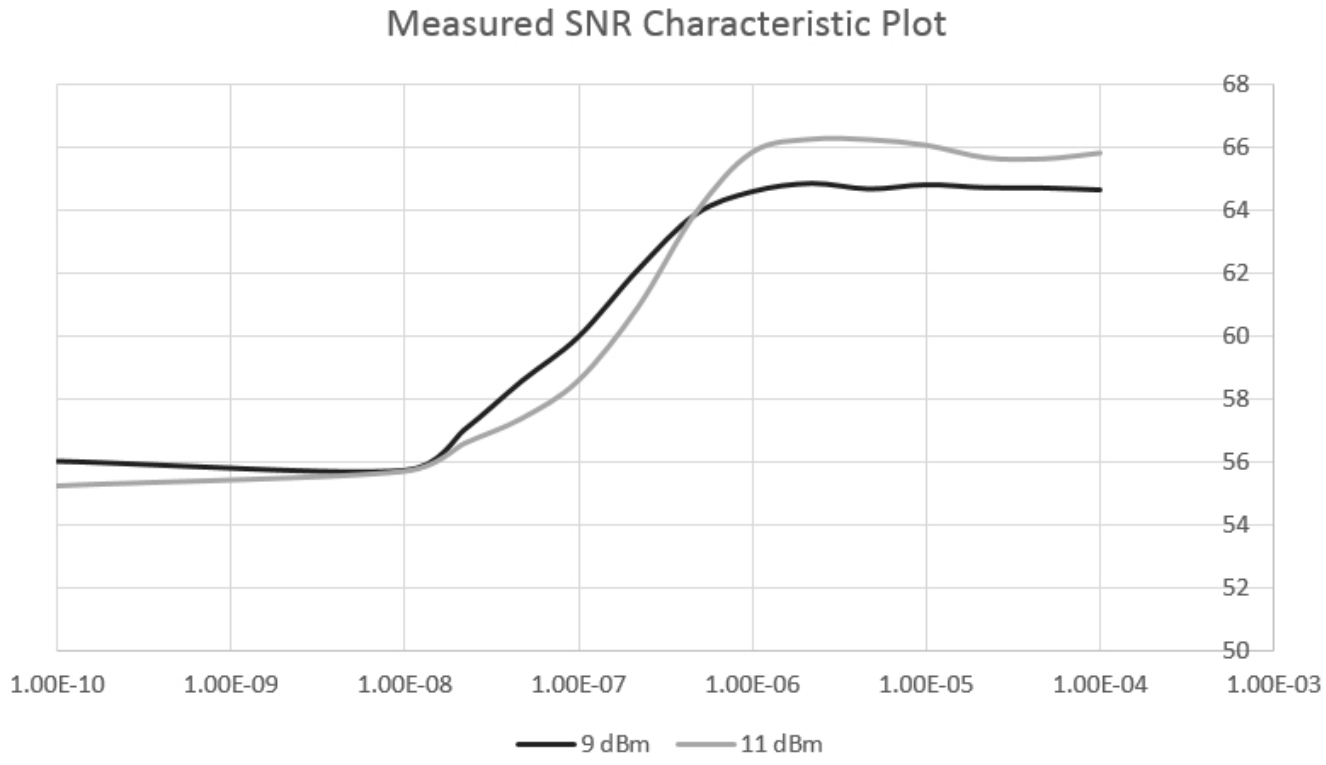


Figure 4.3.6: Measured SNR versus Reference Capacitance for 9dBM and 11dBm Signals

Figure 4.3.7 shows that the two THD curves are on two distinct levels. Both remain relatively constant across the reference capacitance range. This shows that although the first few harmonics are independent of reference capacitance, they are dependent on the amplitude of the signal. This separation does not coincide with the implications of Figure 4.3.3, which shows an inverse relationship between amplitude and THD. As previously discussed, it was known that a higher amplitude input signal set directly on the signal generator led to a higher distortion. However, when the distortion of the signal generator is held constant, decreasing the signal amplitude through filtering causes another source of distortion to increase in power. These distortion terms are mainly limited to the first four harmonics.

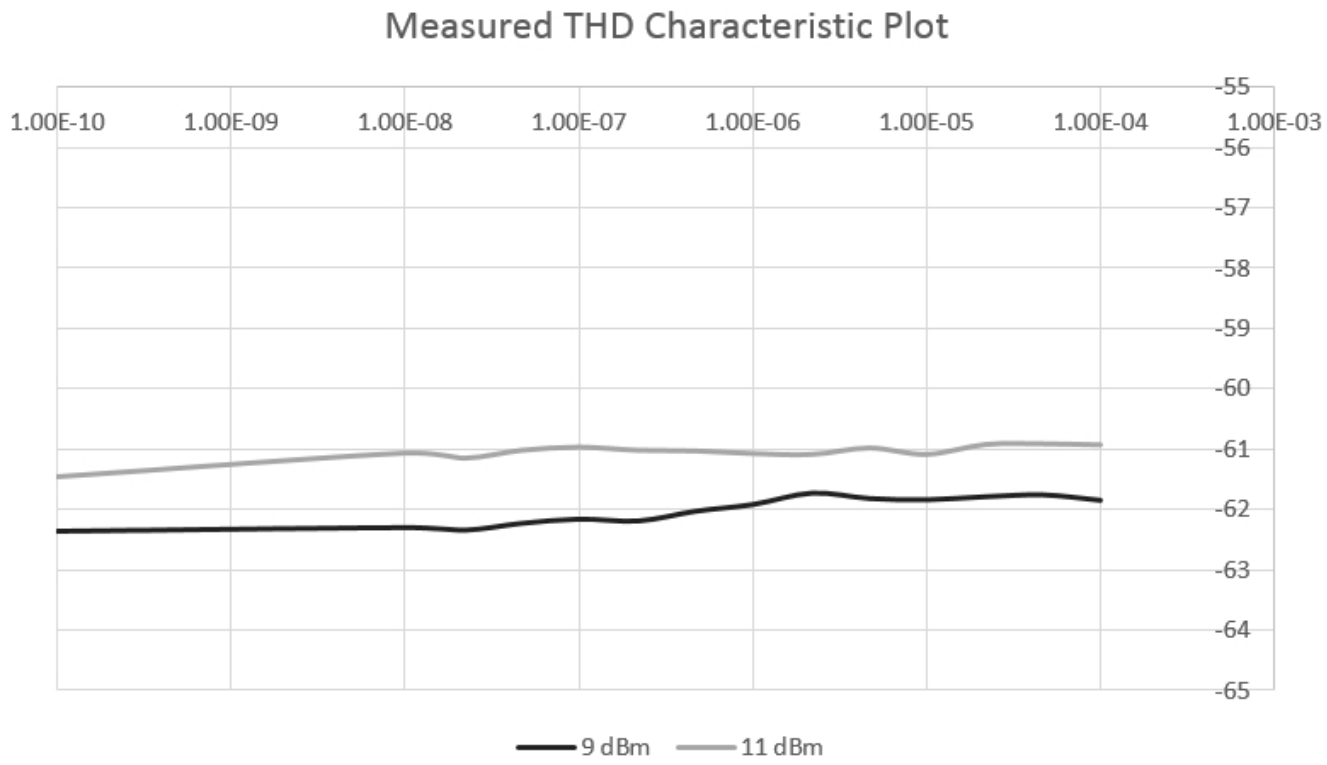


Figure 4.3.7: Measured THD versus Reference Capacitance for 9dBM and 11dBm Signals

Figure 4.3.8 shows that smaller amplitudes will achieve better SFDR. This indicates that although the signal power is lower, the power in the largest harmonic spur decreases even more; which leads to an improvement in SFDR. This finding does not match up with the results illustrated in Figure 4.3.4, which shows the SFDR relationship using constant amplitude set on the signal generator. However, in this case, the change in SFDR implies that the additional distortion power that causes the curves to separate originates from the signal generator itself.

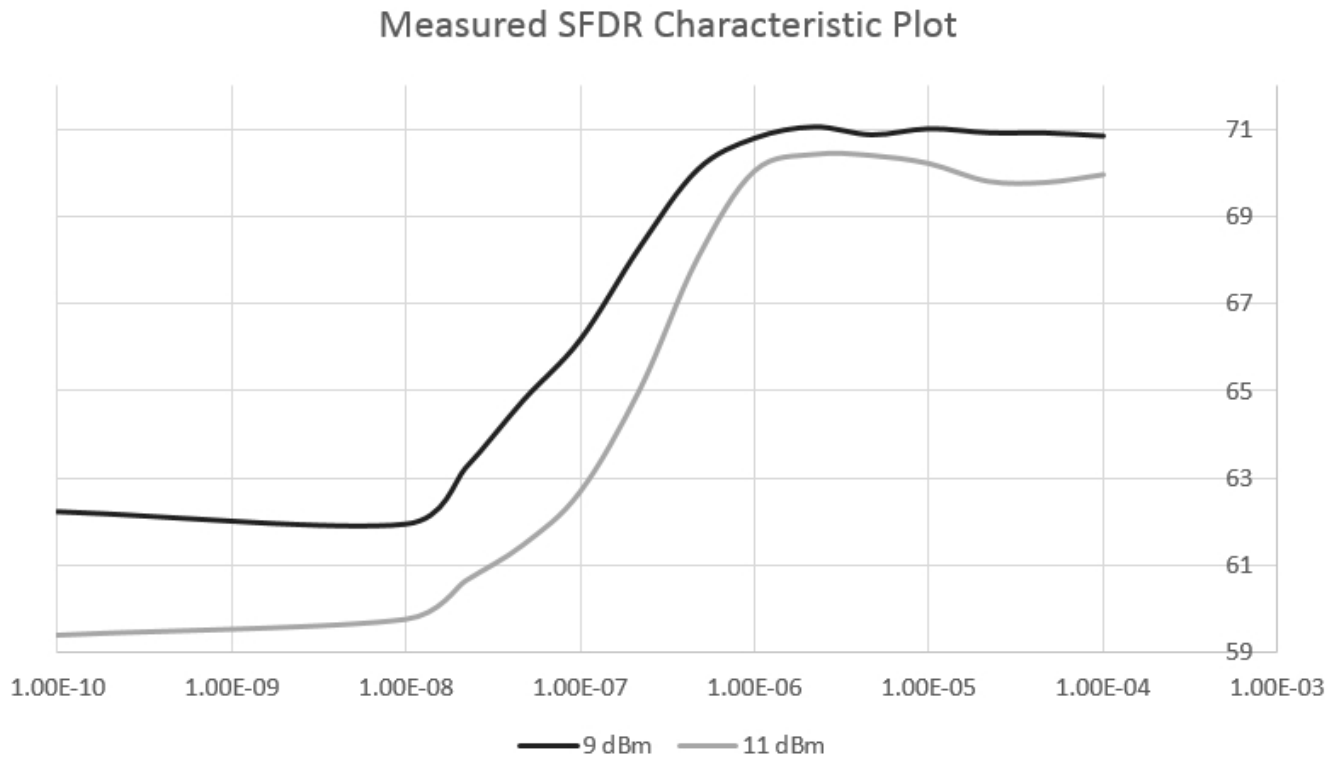


Figure 4.3.8: Measured SFDR versus Reference Capacitance for 9dBM and 11dBm Signals

The measured results presented in this chapter show how the performance of a real ADC varies with different bypass capacitors, or reference capacitances. In the analysis presented in Chapter 3, the bypass capacitor, voltage reference circuit and internal DAC are investigated. However, the analysis ends with a single switching cycle. One measurement taken with controller board contains 2^{17} samples. This implies that the AD7276 completed approximately 2^{20} switching sequences per measurement taken. Thus, it would be too time consuming to complete analytic results to compare with the measured results. Instead, the analysis is used to generate a model programmed in Matlab to generate simulated results. These simulated results are presented and compared to the measured results in the next chapter.

Chapter 5

Simulations

Based on the analysis done in Chapter 3, a model written in Matlab was created. Simulations were conducted using this model to recreate the results seen in the experimental results. The complete code can be found in Appendix H. The AD7276 is a real Successive Approximation ADC (SAR-ADC) with many practical limitations. These limitations include noise, parasitic capacitance, INL and DNL errors, all of which affect the ADC's performance. Since the magnitude of their effect on the performance is unknown to the user, they were not originally considered in the when simulating the simulated sinusoidal signal and the model. Once the ideal simulations were used to generate results, these limitations were identified through comparing the simulations to the measured results.

5.1 Creating a Practical Model

Though the analysis describes how the model should behave, to generate comparable simulated results to the experimental results some additional features were added. Firstly, additional white noise was added to the signal input and output such that the noise floor was at the same level as seen in measurements. Secondly, a parasitic capacitance was added in parallel to the reference capacitor. This was required to shape the response such that the distortion would saturate as capacitance decreases. Without this parasitic capacitor, the distortion would continue to increase in power indefinitely. These added non-ideal components make the simulated model more complete, making it generate realistic, practical results. Additionally this shapes the curve without the need for adding additional distortion terms. Figure 5.1.1 shows a comparison of a SNDR characteristic curve of an ideally realized model to that of the practical results.

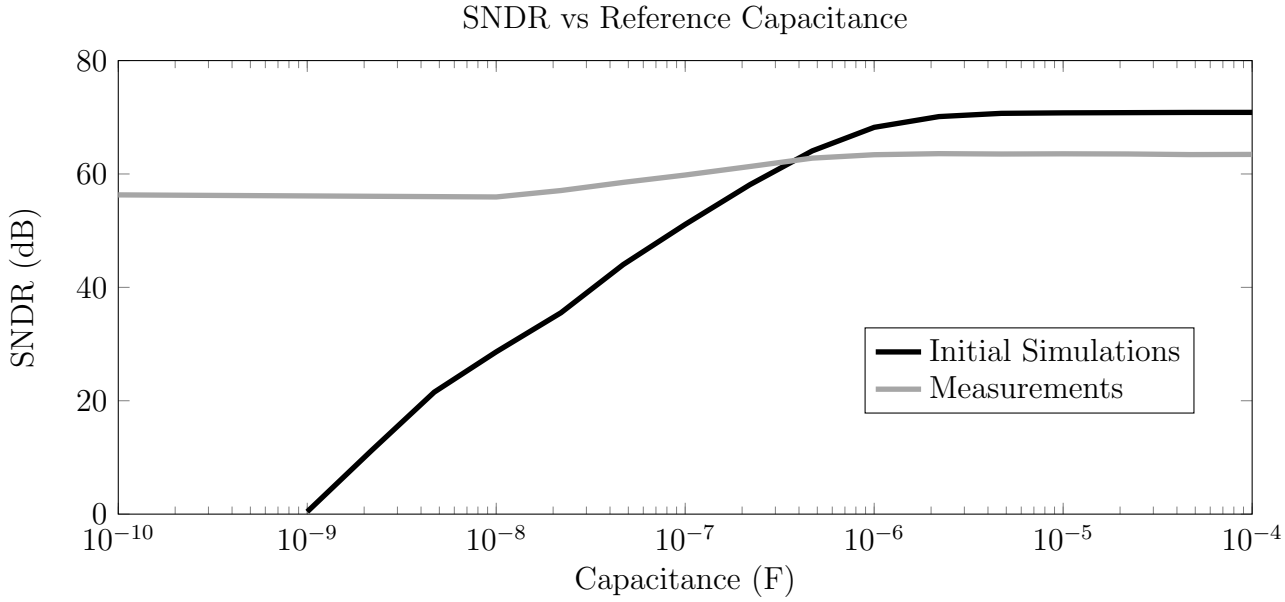


Figure 5.1.1: Simulated SNDR using an Incomplete Simulated Model (Black) versus Measured Results (Grey)

Key factors must be added to the model such that the results coincide with the measured results. Some of which would be noise, parasitic capacitance, and charge restoration of C_{ref}. The noise level for an ideal 12-bit SAR-ADC is derived from Equation 5.1.1 to be at -122dB. It should be noted that N is the resolution of the ADC, and M is the number of bins in the FFT. The Measured results show a noise floor near -100dB, so white noise was added to the input and output sinusoidal signal to model the added noise of the circuit.

$$NoiseFloor = 6.02N + 1.76dB + 10log(M/2) \tag{5.1.1}$$

The AD7276 includes a non-ideal charge redistribution DAC. However, there is no indication of how the internal circuitry is actually implemented. For the purpose of modelling the DAC, many assumptions are made that are incorrect and do not reflect the actual circuit inside. This is done to isolate the non-ideal behaviour being investigated from other circuit dependent issues, and also keep the model simple. In the simulated model, an ideal binary weighted charge sharing DAC was used. Additionally, many assumptions and approximations were made concerning the unit capacitance value for the switched-capacitor array, and the parasitic capacitance previously described. The unit capacitance defines the value for the array capacitance, C_a. Equation 5.1.2 governs how V_{ref} changes, thus by manipulating the ratio $\frac{C_a}{C_{ref}}$ and the parasitic capacitance, the simulated characteristic curve can be shaped. It should be noted that the absolute values of the C_a, C_{ref} and the parasitic capacitance

(C_p) values used for the model are not approximations of the actual values of capacitances in the real ADC. These values were determined for the sole purpose of curve fitting. The analysis done in Chapter 3 shows that the reference errors were proportional to the ratio of the capacitances, not the values of the individual capacitances themselves. Thus, what can be said is that the ratio $\frac{C_a}{C_{ref}+C_p}$ is approximately $\approx 976.5 \times 10^{-6}$.

$$V_{ref,new} = \left(1 - [y(x-y) + z(1-x+y-z)]\frac{C_a}{C_{ref}}\right)V_{ref} \tag{5.1.2}$$

Another assumption being made is how V_{ref} is restored once charge is pulled off of C_{ref}. V_{ref} is decreasing during each switching sequence, however this cannot continue indefinitely. Charge must be pulled from the voltage reference circuit to ensure long-term stability. Many mechanisms were investigated for applicability in the simulated model. Because the purpose of the simulated model is to maintain simplicity in the analysis, only linear and first-order systems were investigated. In one attempt, a constant current source was used to restore V_{ref}. Another attempt involved using a RC first order charge restoring system, where the time to charge the reference capacitor is governed by the RC time constant. These non-ideal charge restorers create a correlation between sampling frequency and the distortion. If there is not enough time for the charge to be restored, then distortion seen at the output should increase as the sampling frequency increases. According to the AD7276 timing analysis, between each sample exist empty clock cycles. This would theoretically allow enough time for V_{ref} to be restored between samples. Furthermore, using charge restoring mechanisms such as the RC system, or simply adding charge proportionally to the difference between V_{ref} and the ideal supply, implies that the reference performs worse, or slower, at higher reference capacitance. According to the measurements, this phenomena is not seen, which implies that sufficient charge is added in between samples to allow V_{ref} to be fully restored. Lastly, since the sampling rate is held constant in this analysis, within a single sample the associated error is relatively constant for each measurement and simulation results. Through simulation, it has been verified that each of the charge restoring mechanisms tested do not show significant differences in their outputs. Thus, to maintain simplicity in the simulation, V_{ref} is simply restored back to its original value after each sample.

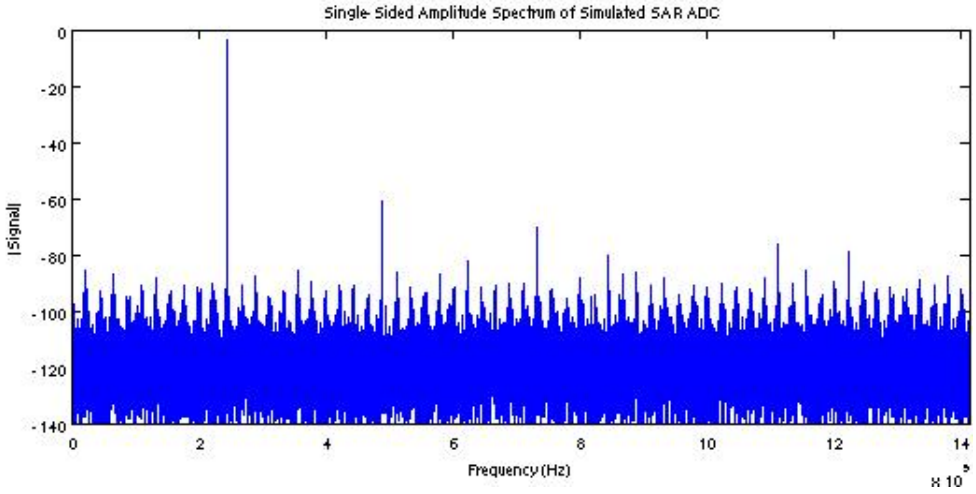
Specifically for the dynamic testing section of this chapter, four different inputs were used. The frequencies and amplitudes of these ideal sinusoidal inputs are the same as those shown in Table 4.2.2. Additionally, the same sampling rate of 20280590 samples per second and 2^{17} samples taken per FFT were used. This was done to provide comparable plots to those seen in Chapter 4.

5.2 Dynamic Testing

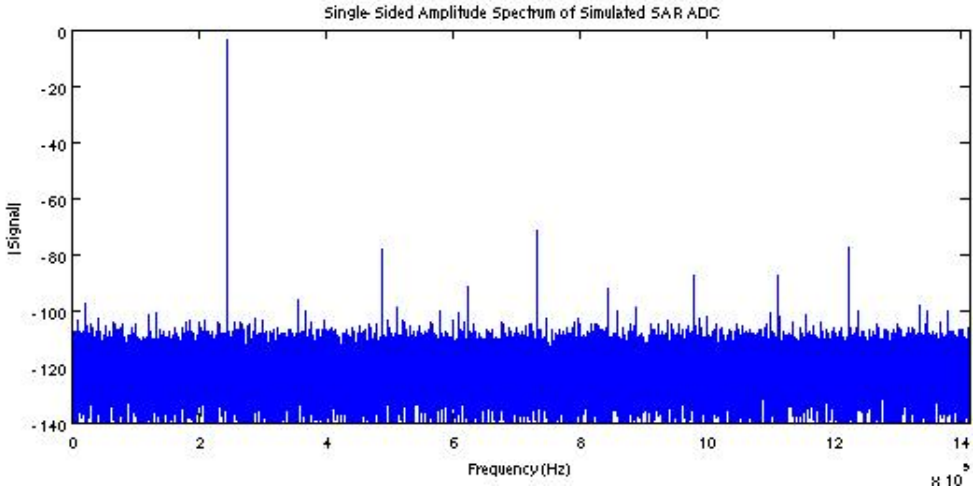
Dynamic testing is used to quantify the distortion seen at the output of the simulated ADC when it is fed an ideal sinusoidal signal. The dynamic specifications taken from the simulations are defined such that they are comparable to the measurements taken in Chapter 4. The dynamic measurements begin with creating of a single tone FFT from the digital output of the simulated ADC.

5.2.1 Simulated FFT Plots

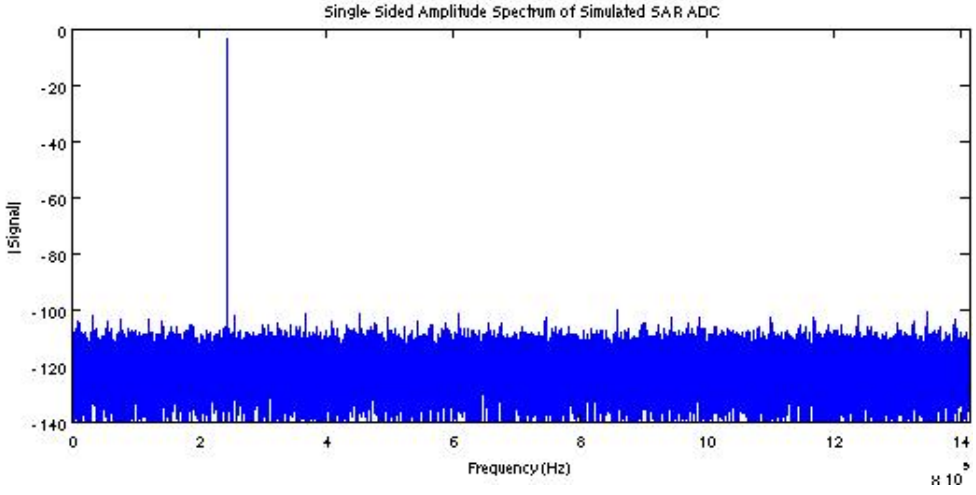
Once the simulated non-ideal ADC provides a digital output, this digital output is ideally converted back into an analog signal. This analog signal is processed using a Fast Fourier Transform (FFT) algorithm to view it in the frequency domain. Figure 5.2.1 shows three FFT plots set up to match Figure 4.2.3. Similarly to that of the measured results, with the $10nF$ FFT harmonic distortion spurs appear throughout the spectrum. When looking at the $0.47\mu F$, we begin to see the first four major harmonics distinctly over the attenuated lesser spurs. Unlike in the measured results, the FFT generated from using a $100\mu F$ reference capacitor shows no significant distortion terms, and is practically ideal. This is because the only source of distortion in the simulated model is from the non-ideal switching and reference capacitor. Thus, the large harmonics seen previously in the measured results are actually generated by other distortion sources. These sources may be part of the signal path within the evaluation board, the power supply coming from the controller board, or caused by the signal generator itself. Additionally, if the AD7276 contains INL and DNL errors due to a practical internal DAC structure, this would not be modelled by the ideal simulated DAC. The reason why the Figure 5.2.1a and 5.2.1b match the measured results is because the distortion was shaped to do so by selecting C_a, noise and parasitic capacitance values to do so. Hence, in simulations the distortion caused by the switching was exaggerated to compensate for the external distortion sources, which were not modelled.



(a) $10nF$ Reference Capacitor



(b) $0.47\mu F$ Reference Capacitor



(c) $100\mu F$ Reference Capacitor

Figure 5.2.1: Three Sample Measured FFT Plots

5.2.2 Calculating Dynamic Specifications

To have comparable results to that of those seen in Chapter 4, the specifications calculated for the simulations must be calculated the same way the evaluation software did for the measured results. These calculations are based on Analog Devices' definitions [17]. In particular, the specifications being calculate are the SNDR, SNR, THD and SFDR.

The Signal to Noise and Distortion Ratio (SNDR) is the ratio of the signal power to the root-sum-square of all the harmonic and noise components.

```
%SNDR
%h(1) is the bin where the input signal is stored
%data is the fft information stored in an array

Signal = 20*log10(data1(h(1)));
data1(h(1)) = 0;   %removes the signal power from the fft data

%subtracts the Signal power from the root-sum-square of all other bins
SNDR = Signal - 20*log10( sqrt ( sum(data1.^2))) ;
```

Figure 5.2.2: Matlab Code to Calculate SNDR

The Total Harmonic Distortion (THD) is the root-sum-square of the first five harmonics. The code to find which bin the harmonics are stored in can be found in Appendix J.

```
%THD
% h is an array that stores the bins where the harmonics are stored
% for example, h(2) stores the second harmonic

total = 0

%Sum the squared power of the first five harmonics
for i=2:6
    total = (data(h(i)))^2 + total;
end
% square root the sum and convert it to decibels
THD = 20*log10( sqrt(total_harmonics));
```

Figure 5.2.3: Matlab Code to Calculate THD

The Signal to Noise Ratio (SNR) is the ratio of the signal power to the root-sum-square of the noise components, excluding the significant harmonics considered in the THD calculation.

```
%SNR
Signal = 20*log10(data1(h(1)));

%Remove the signal and first 5 harmonics from the fft array
for i=1:6
    data1(h(i)) = 0;
end

%subtracts the Signal power from the root-sum-square of all other bins
SNR = Signal - 20*log10( sqrt ( sum(data1.^2)))
```

Figure 5.2.4: Matlab Code to Calculate SNR

Finally the Spurious Free Dynamic Range (SFDR) is the ratio of the signal power and the next largest spur in the FFT plot.

```
%SFDR

Signal = 20*log10(data1(h(1)));
data1(h(1)) = 0;    %removes the signal power from the fft data

[worst_spur, tmp] = max(data1(:)); %Finds the magnitude of the worst spur
SFDR = dB_data(fa) - 20*log10(worst_spur);
```

Figure 5.2.5: Matlab Code to Calculate SFDR

Using the definitions of the dynamic specifications provided by Analog Devices, the measured and simulated results can be compared fairly.

5.2.3 Simulated SNR , SNDR, THD, and SFDR vs Capacitance

The data presented in this section of the chapter should be compared to section 4.3. The purpose of generating simulated plots is to demonstrate that the simulated model correctly describes the distortion behaviour seen in the characteristic curves taken from measurements.

The Simulated SNDR Characteristic

Figure 5.2.6 shows the simulated SNDR versus reference capacitance plot. Similar to the measured results, the curve shows the characteristic S-shape with the SNDR saturating at around 66 dB for high capacitance and around 55 dB for low capacitance. Additionally, the SNDR rises exponentially between $10nF$ and $1\mu F$. The higher corner point, or inflection point, on the curve emerges from Equation 5.1.2. While C_{ref} is sufficiently larger than C_a, the change in V_{ref} is too small to affect the ADC's linearity. As C_{ref} decreases, the change in V_{ref} approaches V_{LSB}, which causes the SNDR to deteriorate. V_{LSB} is defined in Equation 2.2.2. If the error in V_{ref} approaches V_{LSB}, the SAR-ADC will incorrectly resolve an output code. As discussed earlier, the second lower corner of the characteristic S-shape where the SNDR saturates at lower capacitance comes from the parasitic capacitance added into the model. The saturation levels and corner points were manipulated by selecting C_a and the parasitic capacitance values such that the results specifically match those from the AD7276. This is true in the analysis of the other simulated results discussed in this section.

It should be noted that the simulated values for C_a and parasitic capacitance do not accurately describe the capacitances within the AD7276 and evaluation board. The values were selected for curve fitting purposes using the assumptions in the ADC's architecture. However, the ratio $\frac{C_a}{C_{ref}}$ is relevant since it determines the amount of distortion, or error. Refer to Section 5.3 for further information on the verification of the simulated model.

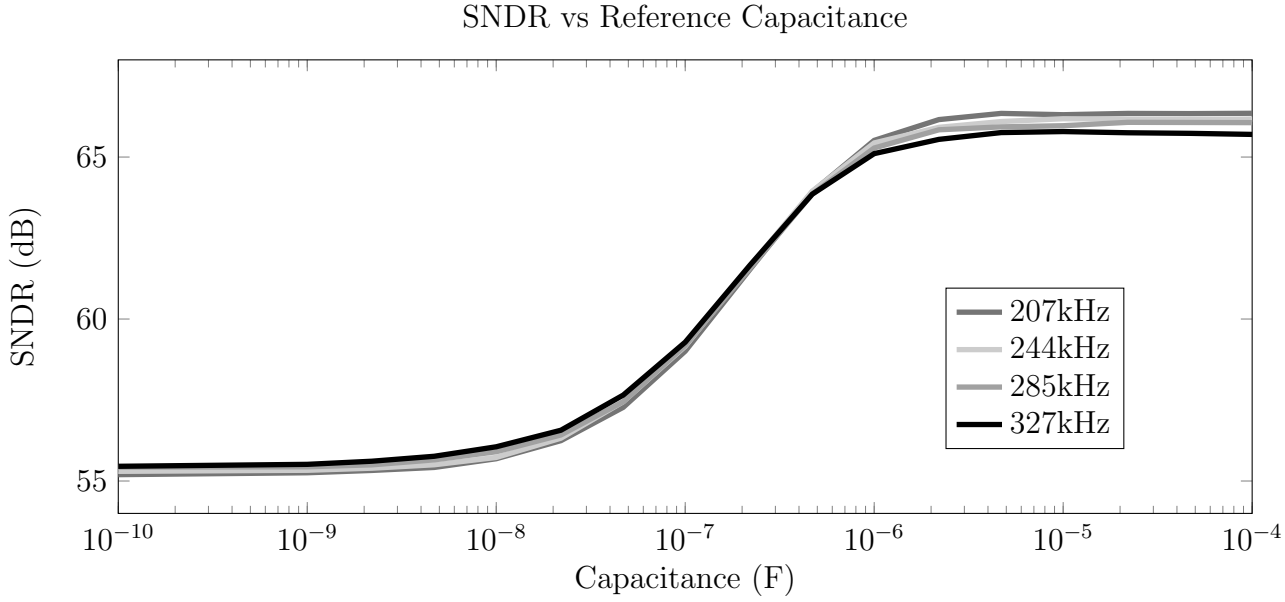


Figure 5.2.6: Simulated SNDR vs Reference Capacitance

The Simulated SNR Characteristic

The SNR relationship, seen in Figure 5.2.7, also has the characteristic S-shape. This implies that the noise level is dependent on the reference capacitance value. This result, however, is misleading. The simulated model of the ADC does not include modelled noise sources in the design, since the components within the model are ideal. Though the SNR begins to deteriorate at lower capacitance, the actual noise floor does not change, as it is defined by the added white noise. The distortion caused by perturbations in the reference voltage increases at lower capacitance as defined by Equation 5.1.2. As seen in Figure 5.2.1, these non-ideal perturbations cause distortions that spread throughout the frequency spectrum. In the algorithm to define SNR, only the first few harmonics are omitted, however the simulation adds all other harmonic tones. These tones continue to alias, filling the FFT. The SNR algorithm does not differentiate between these distortion terms and noise. Since all the distortion is correlated with C_{ref}, the SNR plot shares the same characteristic S-shape as the SNDR plot.

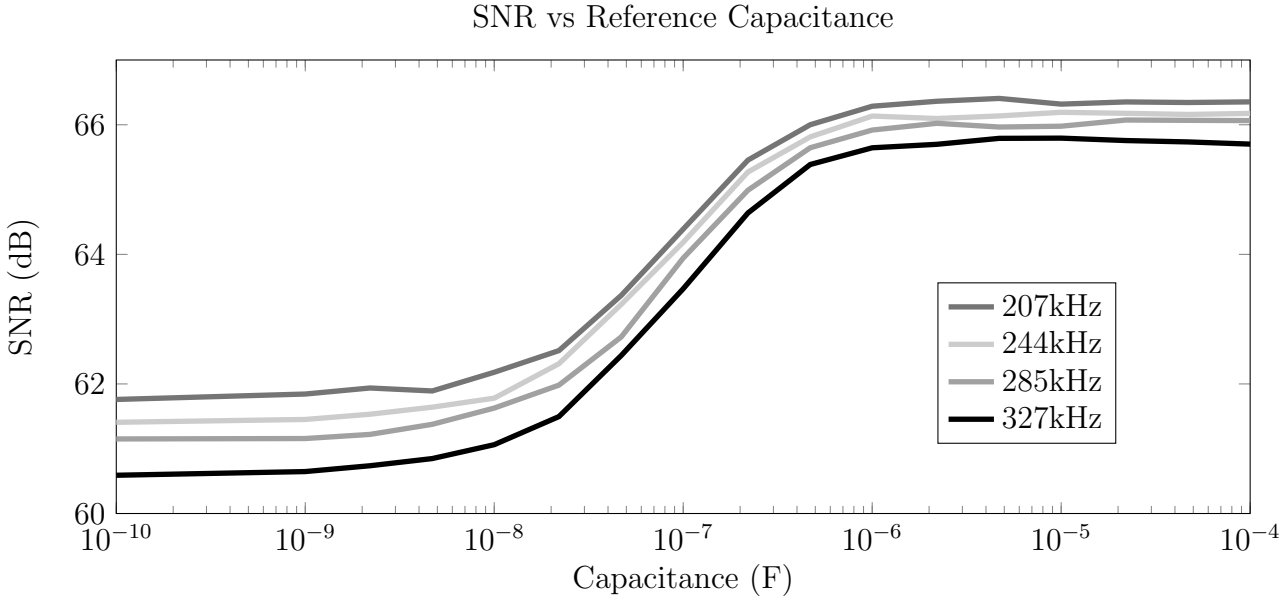


Figure 5.2.7: Simulated SNR vs Reference Capacitance

The Simulated THD Characteristic

Figure 5.2.8 shows the THD versus reference capacitance characteristics. As mentioned earlier, the distortion power increases exponentially with decreasing capacitance. The reason why the THD saturates at low capacitance is due to the parasitic capacitance added into the ADC's simulation model. If this parasitic capacitor was not in the model, the THD would not saturate and continue to increase in magnitude. At high capacitance the THD continues to decrease exponentially until it saturates at around -100dB. This is the point at which the harmonic distortion power is lower than the noise power. Since the noise is random, the THD curve is not smooth in this area of the graph.

The simulated THD graph does not match with Figure 4.3.3 of the measured results. The reason being that the distortion within simulations only originates from the non-ideal switching and reference capacitor. The distortion from this source follows the curve shown in Figure 5.2.8. This THD curve coincides with the S-shaped characteristic curves of the SNDR and SNR plots. The measured results show a relatively constant THD curve, which implies the harmonic distortion is independent of the reference capacitor. This is because external distortion sources have hidden the distortion caused by the switching, as discussed in the previous Section 5.2.1.

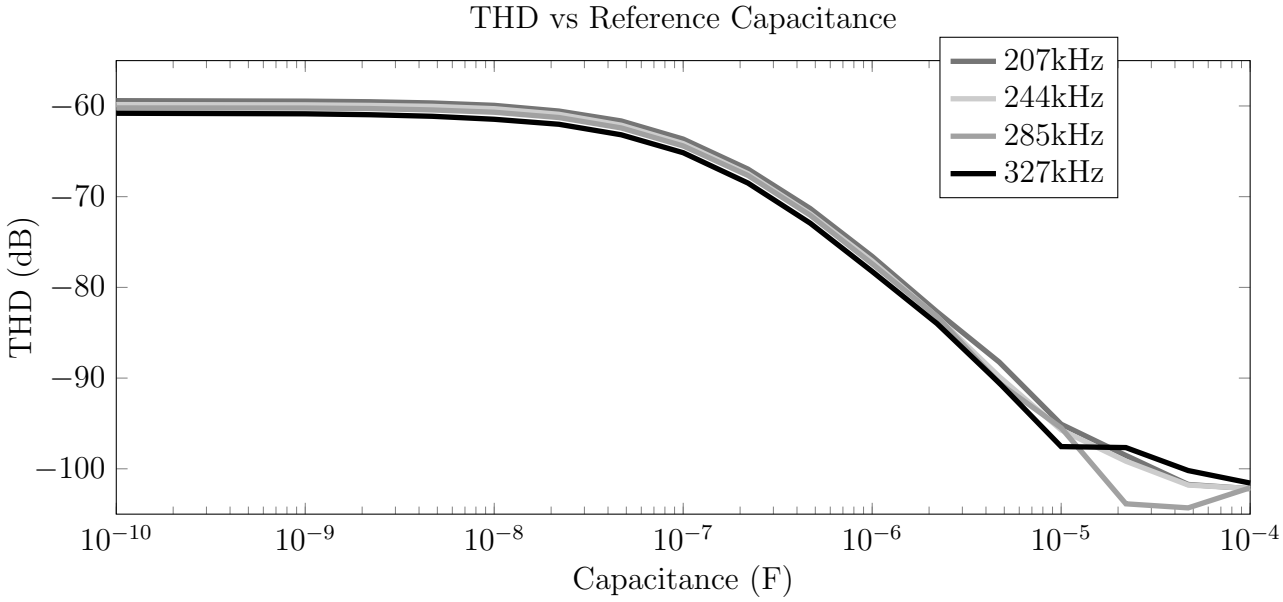


Figure 5.2.8: Simulated THD vs Reference Capacitance

The Simulated SFDR Characteristic

The SFDR plot is shown in Figure 5.2.9. As previously defined, the SFDR is the difference between the signal power and the largest spur. In the simulations, the largest spur is always the second harmonic. This is one occasion where the simulated plot does not compare with the measured plots. In measurements the SFDR was limited by a distortion spur near the fifth harmonic. That being said, since the second harmonic spur is coherent with THD, the SFDR plot shows what looks like an inverted THD curve.

The simulated SFDR illustrates a much better response compared to the measured SFDR plot due to the fact that at large reference capacitance, the output signal is almost ideal. However, the measured results still contain harmonics independent of C_{ref} within the spectrum which can be seen in Figure 4.3.3. These independent harmonics were not added to the simulation since it would hide the distortion the thesis is primarily concerned with.

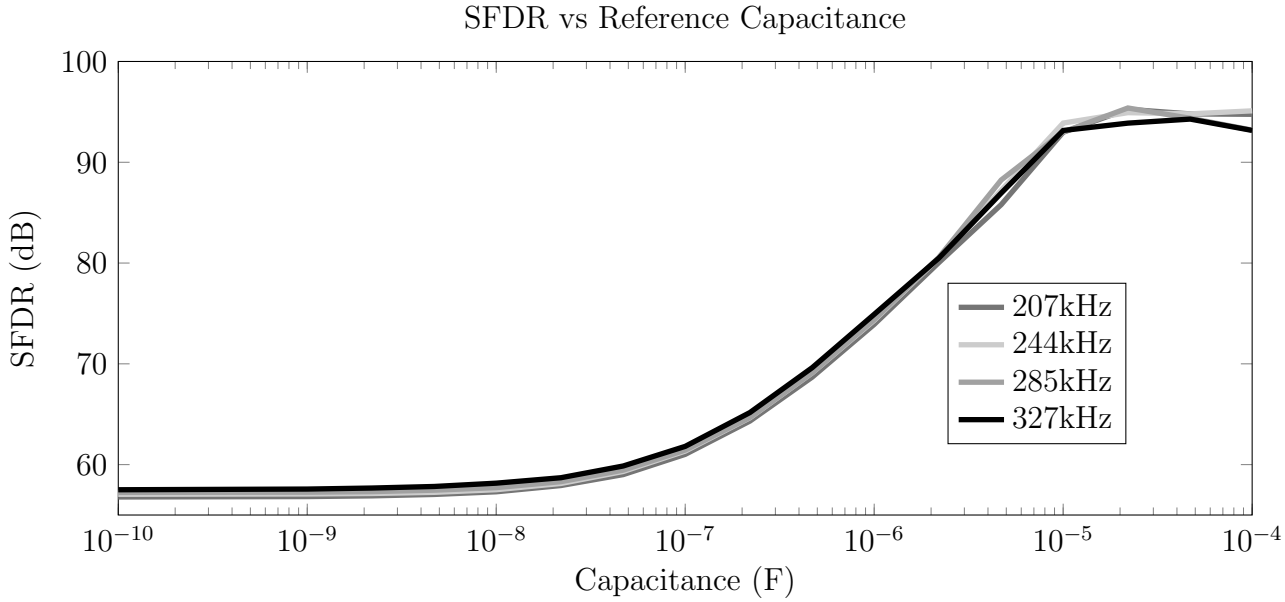


Figure 5.2.9: Simulated SFDR vs Reference Capacitance

5.3 Time-Domain Error Analysis

The distortion seen in the FFT plots originates from errors generated during quantization. Comparing the errors generated through simulation to those measured through experimentation will add an additional degree of validity to the simulated model. The simulation of the modelled ADC begins with feeding an ideal sinusoidal signal into the input, just as a

sinusoidal signal was used as an input for the lab measurements. The simulated sinusoidal input is divided into the same number of samples used for measurements; approximately three million samples. Each sample is individually quantized to create a digital output. Then, the binary output is digitally converted into decimal and scaled to recreate the input signal. The difference, however, is that the output signal now includes the quantization noise and distortion added during the quantization process.

By subtracting the ideal input signal from the reconstructed output signal, the absolute error can be calculated. This error is viewed in the time domain. A similar error calculation can be done with the measured results. By comparing the measured error with the simulated error, the validity of the simulated model is checked. In Figure 5.3.1 below, we see the comparison of the worst case errors due to using a small reference capacitance. In this figure, the bottom signal represents the ideal sinusoidal output used as context for the error lines.

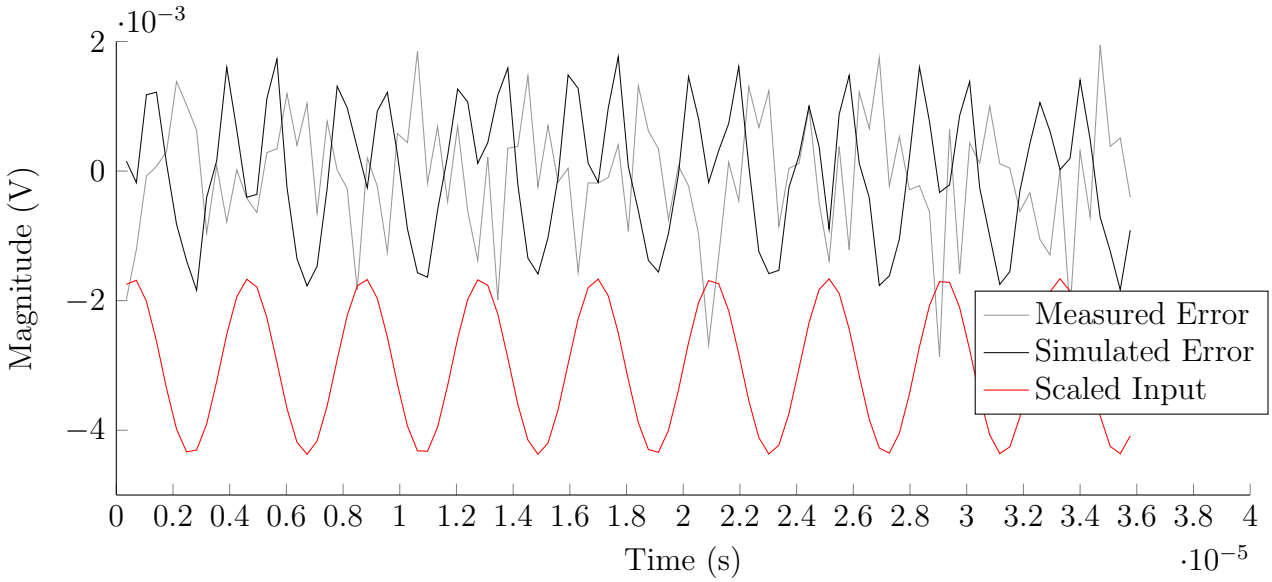


Figure 5.3.1: Time Domain Comparison of Measured and Simulated Errors using a $10nF$ Reference Capacitor

It is important to note that the switching sequence and array structure of the AD7276 SAR-ADC used in measurements is not the same as what is used in the simulated model. The simulated model uses a basic binary weighted array with a standard successive-approximation algorithm. Because of these simplifications, the values for the unit and parasitic capacitances do not correctly reflect the actual internal values within the actual AD7276 chip. However, since the values of C_{ref} used in the simulated model and in the experiment are the same and because the errors from measurements and simulation are similarly bounded, the simulated ratio $\frac{C_a}{C_{ref}}$ is comparable to the ratio of the real components. It is noted that the shape of the

errors do not match because the switching sequence and array architecture do not match.

Figure 5.3.2 displays the error using a large reference capacitor. This compares the best case errors for the simulated and measured results. The simulated error is significantly smaller than the measured error. This is expected since it is presumed that there are harmonics from other distortion sources. This external distortion source is not modelled in the simulation.

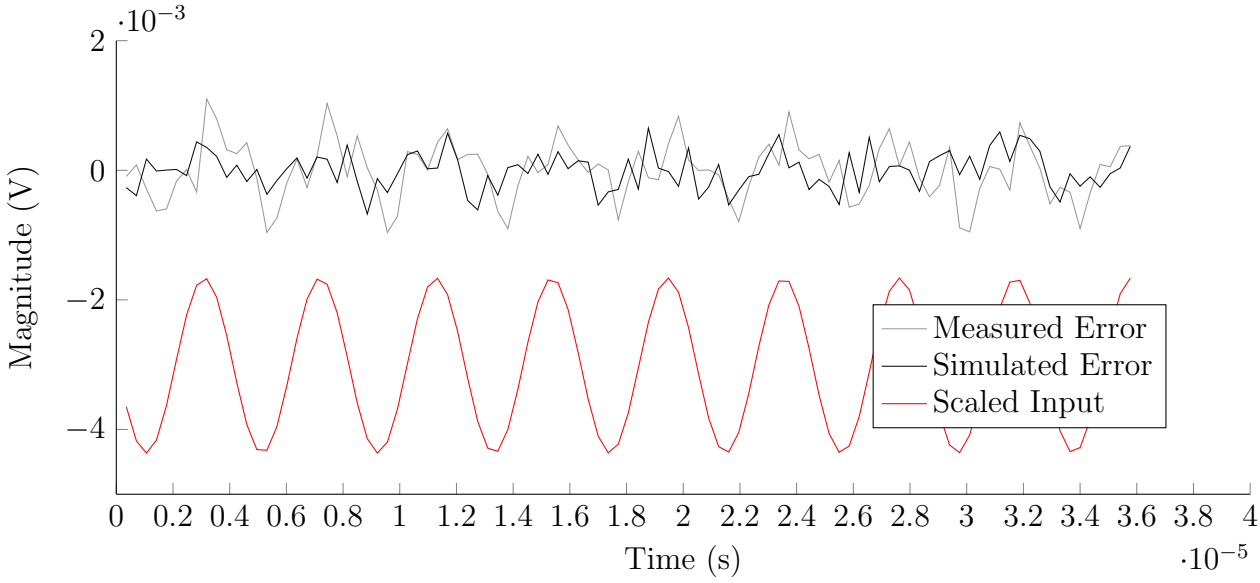


Figure 5.3.2: Time Domain Comparison of Measured and Simulated Errors using $100\mu F$ Reference Capacitor

5.4 Static Testing

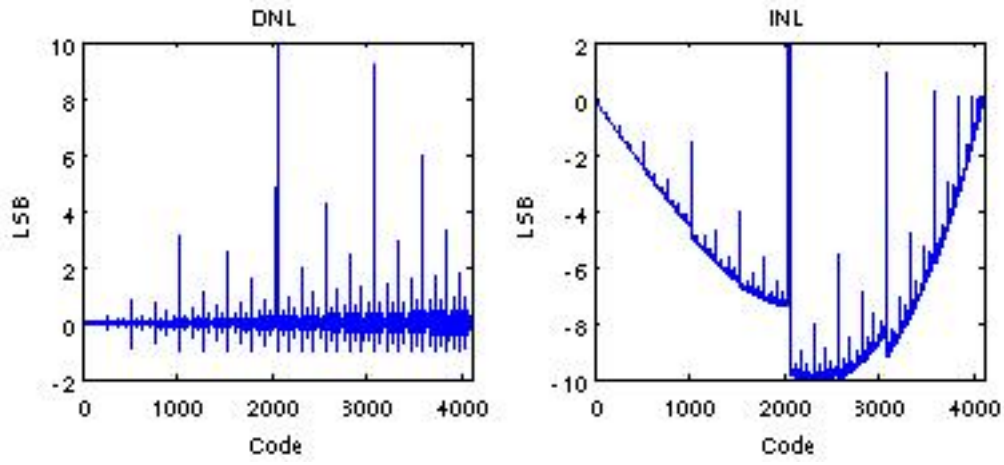
Static testing is done by putting a high resolution ramp as the input to the simulated ADC. Since the data being tested comes from a simulated model there are no offset or gain errors. The relevant specifications calculated are the linearity errors, namely differential non-linearity (DNL) and integral non-linearity (INL). Due to limitations in the measurement process, the INL and DNL readings were not taken from the AD7276 development board. One such limitation is that due to attenuation along the signal path, an undistorted full-scale signal could not be applied at the input of the ADC. Thus, there is no comparison between the measured and simulated results in this case. However, because the simulated model is based on an architecture and switching sequence that does not match the AD7276, it would be difficult to draw any relevant conclusions from such a comparison.

The DNL is found by putting an ideal ramp through the ADC. The resolution of the ramp is 100 times the resolution of the ADC. Ideally, the output of the ADC should show each

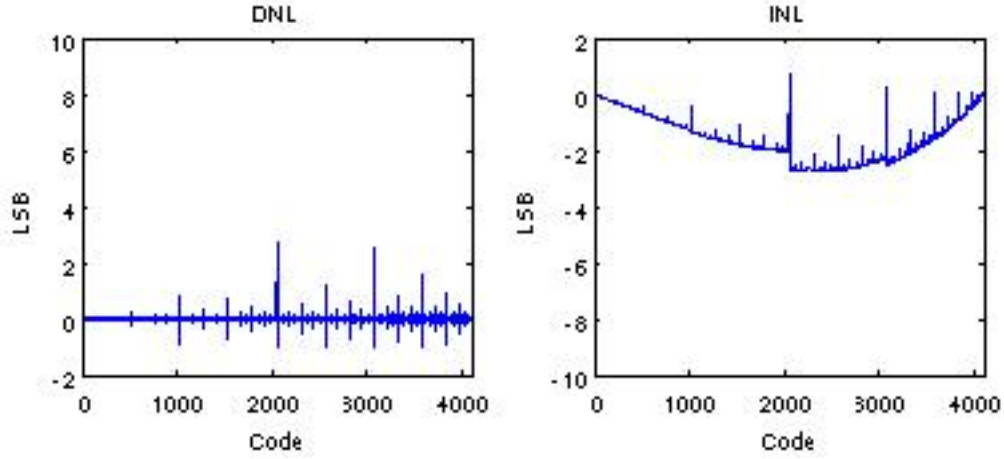
code 100 times. Due to linearity issues, the codes will show a variation in their count. The DNL of that code is the measured count minus the ideal count. Once the DNL is calculated, the INL can be easily calculated. The INL is simply the rolling sum of the DNL [4].

The INL and DNL plots can be used to gain insight to the simulated model's performance and to verify the dynamic testing results. Figure 5.4.1 shows the DNL and INL plots for a small reference capacitor, a large reference capacitor and an intermediate reference capacitor. It is seen that at low capacitance, the nonlinearity is significantly high, with a maximum INL of 10 LSB. When looking at the $1\mu F$ reference capacitor plot, it is seen that the shape of the DNL and INL plots remain the same. However, the magnitude of the errors decreases significantly. This continues as the reference capacitance increases until the nonlinearity effectively disappears, as shown in Figure 5.4.1c. Additionally, An INL of 1 LSB is achieved using a $1.3\mu F$ reference capacitor.

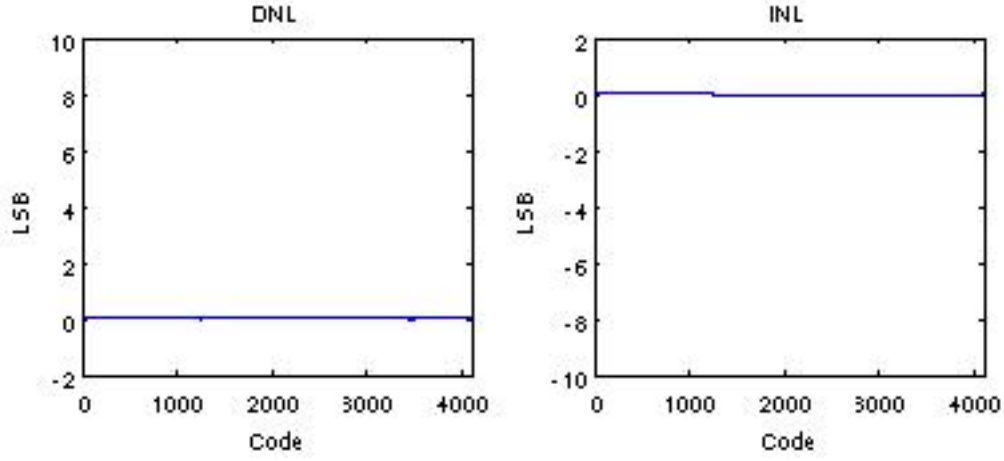
One characteristic from these plots is that smaller codes, on average, have lower DNL than the higher codes. When looking at the dynamic specification plots, such as SNDR, there is a small separation between the four inputs tested. The reason of this separation can be explained by the slight variations in amplitude of the four inputs. The signals with higher amplitude invite higher distortion into the signal. This also can be used to verify that in simulation, the difference in distortion level across the four inputs is amplitude dependent and not frequency dependent.



(a) $10nF$ Reference Capacitor



(b) $0.47\mu F$ Reference Capacitor



(c) $100\mu F$ Reference Capacitor

Figure 5.4.1: Three Simulated INL and DNL plots

The worst case INL is a good measure of an ADC's distortion. Figure 5.4.2 shows how the worst case INL relates to reference capacitance. Though it does not provide as much information as a full INL plot, as seen in Figure 5.4.1, it provides ample information regarding the worst errors due to distortion. The INL curve is very similar to the THD characteristic as it shows a rapid increase in distortion near the $1\mu F$ reference capacitance mark.

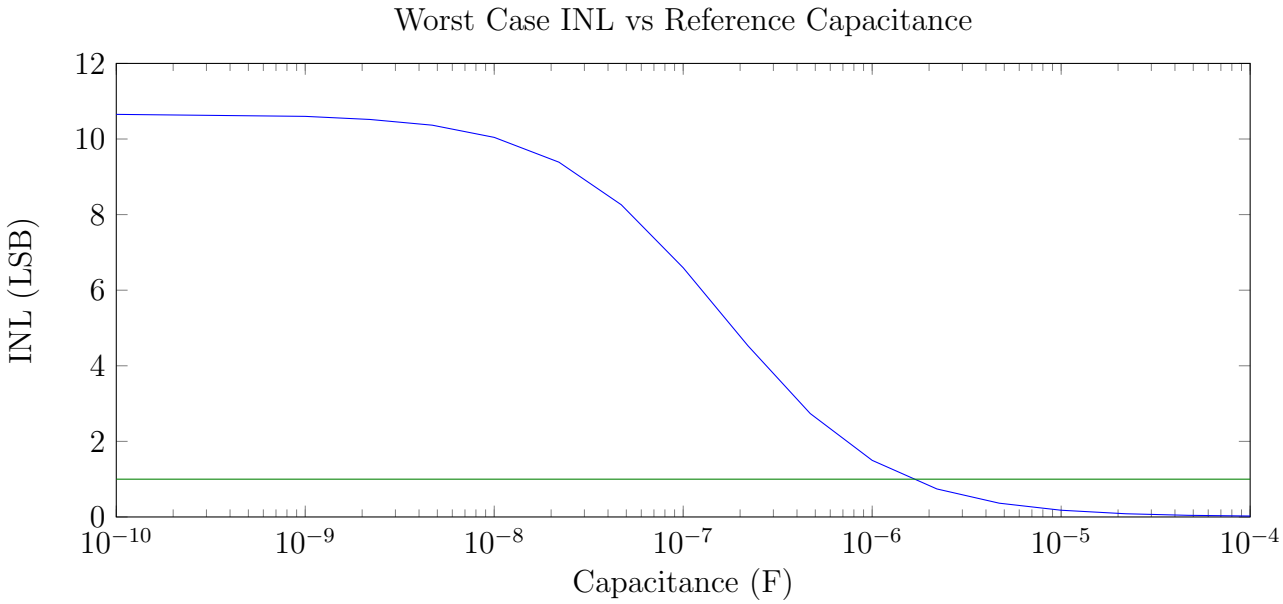


Figure 5.4.2: Simulated THD vs Reference Capacitance

Another indication of distortion in static testing is the existence of a missing code. A worst case DNL of -1 LSB or lower implies that there is atleast one missing code. A missing code is a code within the digital output range that cannot be outputted by the ADC for any analog input. This is a form of distortion since the occurrence of the missing code is not random. Furthermore, Figure 5.4.3 shows how the worst-case DNL changes with regards to reference capacitance. Additionally, the DNL never drops below the -1 LSB threshold.

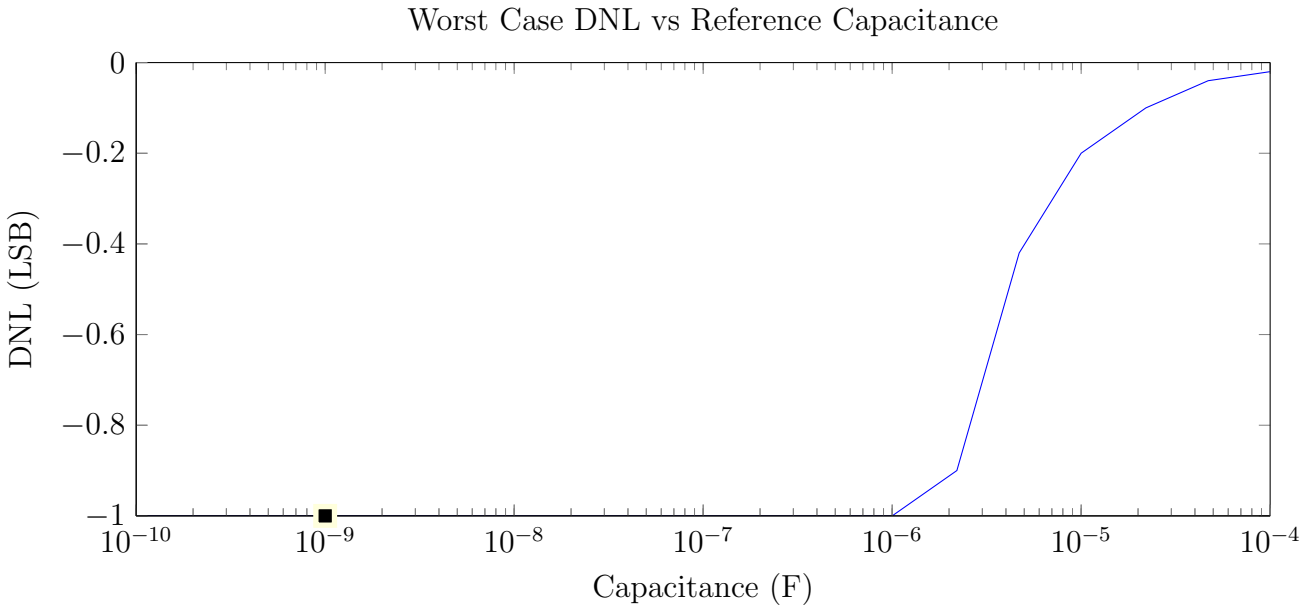


Figure 5.4.3: Simulated THD vs Reference Capacitance

In simulation, the INL curve crosses the threshold at a reference capacitance of $1.6\mu F$. The INL then increases quickly as the reference capacitance decreases, keeping in mind that the x-axis shown in Figure 5.4.2 is logarithmic. The DNL curve shows the DNL reaching -1 LSB at approximately $1\mu F$.

Chapter 6

Conclusion and Discussion

This thesis investigated distortion generated within the Successive Approximation ADC (SAR-ADC) due to a non-ideal voltage reference. The source of distortion was found to stem from the interaction between the analog circuit within the SAR-ADC, the internal digital to analog converter (DAC), the voltage reference circuit and the bypass capacitor used for decoupling their connection. Through circuit analysis, the distortion due to a non-ideal voltage reference was found to be proportional to the ratio of the capacitance of the internal DAC to the capacitance of bypass capacitor. This analysis was tested through lab measurements, where the bypass capacitor was varied and different distortion specifications were measured. The characteristics generated through the measured results reinforce the findings found through analysis. A simulated model based on the analysis done in this thesis was created. This simulated model was used to generate characteristics that matched those of the measured results. This further verifies that the simulations, and the analysis, correctly model the behaviour of the real circuit.

A practical SAR-ADC used today include a robust bypass capacitor, which has been found to be excessive. The stock bypass capacitor for the AD7276 evaluation board is $10.1\mu F$, and can be higher in other SAR-ADC systems. Through measurements it is seen that a reference capacitor, or bypass capacitor, of $1\mu F$ can be used without a significant loss in performance. This is the minimum reference capacitance before the distortion begins to grow exponentially. Thus, by making the capacitor one order of magnitude smaller, the SNDR will still remain maximized and the effective number of bits will remain the expected value. By reducing the reference capacitor size, a designer can see cost and space savings regarding the usage of the SAR-ADC. Furthermore when looking at a fully integrated circuit solution, an order of magnitude reduction in capacitance will lead to an order of magnitude savings in die area. To verify these findings, a generalized model of the bypass capacitor and the SAR-ADC's internal DAC was examined.

The simulated model was based on a simplified SAR-ADC architecture and switching sequence whose non-ideal switching causes charge to be pulled off of the reference capacitor. As charge is pulled off the reference capacitor at N times the sampling rate of the ADC, perturbations in the reference voltage lead to distortion at the output of the ADC. The final conclusion of the analysis can be seen in Equation 6.0.1. Based on this theoretical model, simulated characteristic curves were created to compare with the measured results. From the simulations, we see that a reference capacitance of approximately $1.6\mu F$ allows for an INL error of 1 LSB. From the dynamic testing plots, it can be approximated that $1\mu F$ capacitance will not significantly lead to a drop in SNDR compared to a larger capacitor. This result matches that of the measured results. Though the simulated model was designed to match the specific case of the AD7276, the importance of the model is that the ratio of $\frac{C_a}{C_{ref}}$ can be modified to match other SAR-ADCs. It should be noted that if the internal array capacitance is known and the parasitic capacitance measured, the designer can size the reference capacitance according to the analysis outlined in this paper.

$$V_{ref,new} = \left(1 - [y(x-y) + z(1-x+y-z)]\frac{C_a}{C_{ref}}\right)V_{ref} \tag{6.0.1}$$

In reality the AD7276 switching sequence is not the simplified algorithm presented in Chapter 3, nor is the the internal DAC a binary weighted capacitive array. However, the simulation results show a magnitude of error in the output comparable to, and in the same order of magnitude, the measured error. The main difference between the simulated and measured results is that the measured results include additional external sources of distortion. Thus the charge being pulled off of V_{ref} cannot be assumed to be in the same magnitude. This implies that the distortion viewed in the simulated plots has been over-compensated to match the multiple distortion sources seen in the measured results. Because of this, the THD curves between the two systems do not match. However, it is expected that the distortion caused by the non-ideal switching and bypass capacitor follows Figure 5.2.8. Though the distortion is hidden by harmonics originating outside of the ADC, the smaller distortion terms react similarly to changes in reference capacitance. This can be seen by viewing the change in the smaller distortion spurs in Figures 4.2.3 and 5.2.1. Because of this, the shape of the SNDR, SNR, and SFDR curves show the S shaped characteristic in both the measured and simulated plots. Hence, even though the external distortion overpower the first four harmonics within the measured results, the analysis used in the simulated model was verified and the conclusions are relevant.

During experimentation and measuring, different directions of analysis were identified for potential future work and opportunities for improvement. Firstly, the future work would include methods to improve the testing method and results. This would include finding

equipment and software. Secondly, further characterizing the bypass capacitor and voltage reference circuit can be done to gain a higher level insight into the observed non-ideal behaviours. Lastly, by applying the analysis done in this thesis further, a higher level model can be investigated. Any of these directions can lead to improvements in the findings of this thesis.

Improving the equipment used to take measurements of the SAR-ADC would improve the reliability of the results, and reinforce the found conclusions. One such improvement would be to design a board or modify the existing evaluation board such that the input from the signal generator can be fed directly to the ADC. This would reduce sources of distortion along the signal path prior to reaching the ADC itself. Additionally, this would allow for full-scale testing of the ADC. Secondly, the signal generator and the evaluation board's clock were not synchronized during measurements. To get around this problem, software used to collect the data utilized a Blackman-Harris windowing function to generate the FFT plot. However, a better solution for future work would be to use different instrumentation that would include clock generators, which can be used to achieve coherent sampling. The clock generator would be used generate the internal clock of the controller board and the evaluation board, provide the chip select signal for the AD7276, and act as a synchronizer for the signal generator. Lastly, a board that can allow for the testing of a variety of SAR-ADC ICs with the same (or similar) inputs and outputs can be used to verify that the findings can be generalized to the SAR-ADC regardless of the internal architecture.

Future work can be done to further characterize the bypass capacitor and how it relates to output distortion. This thesis simplifies the bypass capacitor and the voltage reference circuit as a single charged capacitor. A more detailed model could be used to explain the unexpected results found. During experimentation, smaller capacitors of $4.7nF$ and $2.2nF$ were used. However, these capacitors were not of the same package as the rest due to availability. Their results were inconsistent with the rest of the measurements, such that the distortion was reduced in comparison to using a $10nF$ capacitor. Thus using the smaller packaging improved the overall performance of the system. Future investigations could include how the ESR and ESL of the reference capacitor affects the performance of the ADC. Additionally, bond wire inductance can be added to the model for further accuracy of the model. An assumption made during the analysis was that the reference capacitor fully-charged between samples. By investigating how charge is restored and how it relates to the reference capacitor, a maximum sampling clock rate can also be identified.

Lastly, this paper ended its circuit analysis where the change in V_{ref} was identified per switching sequence. For future work, analysis into finding a direct relationship between $\frac{C_a}{C_{ref}}$ and the dynamic measures, such as SNR and THD, can be found to remove the need for simulations. This would be considered a higher model of the entire system, which can be

used to estimate the performance of the ADC prior to fabrication or assembly.

All this work and the future directions which this thesis can take can be used to work towards the research of a fully integrated SoC solution which integrates the SAR-ADC and the voltage reference within its parent integrated circuit. This paper is based on board level measurements and experimentation. However, the generalized model used to characterize distortion can be applied to an integrated circuit setting. Similar measurement and analysis of an IC based SAR-ADC system can be carried out to verify if the distortion is proportional to the $\frac{C_a}{C_{ref}}$ ratio. Through the application of the findings of this thesis, the capacitors required to implement the integrated SAR-ADC with sufficient decoupling can be efficiently sized to meet distortion requirements.

Appendices

Appendix A

Alternate Calculation for Finding ΔQ

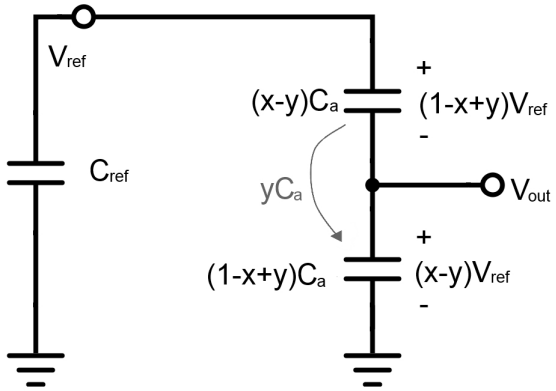


Figure A.0.1: The y switching sequence for the simplified model

Here we originally see three capacitors in the array, $(x-y)C_a$, $(1-x)C_a$ and yC_a. In this calculation we are only considering the bottom part of the array, which include $(1-x)C_a$ and yC_a. It should also be noted that as yC_a is moved from the top capacitor array to the bottom, its polarity switches.

For the $(1-x)C_a$ capacitor:

$$\Delta V = V_{final} - V_{initial} \tag{A.0.1}$$
$$= (x-y)V_{ref} - xV_{ref} \tag{A.0.2}$$
$$= -yV_{ref} \tag{A.0.3}$$
$$\Delta Q = \Delta V(1-x)C_a \tag{A.0.4}$$
$$= (xy-y)C_aV_{ref} \tag{A.0.5}$$

For the yC_a capacitor moving from top to bottom:

$$\Delta V = V_{final} - V_{initial} \tag{A.0.6}$$
$$= (x - y)V_{ref} - [-(1 - x)]V_{ref} \tag{A.0.7}$$
$$= (1 - y)V_{ref} \tag{A.0.8}$$
$$\Delta Q = \Delta V y C_a \tag{A.0.9}$$
$$= (y - y^2)C_a V_{ref} \tag{A.0.10}$$

By combining both results we see that:

$$\Delta Q_{total} = (xy - y)C_a V_{ref} + (y - y^2)C_a V_{ref} \tag{A.0.11}$$
$$= (xy - y^2)C_a V_{ref} \tag{A.0.12}$$

This is exactly the same ΔQ previously found by only considering the simpler case of the top capacitor array. Thus, only one calculation is needed, and the simpler case is used.

Appendix B

Accurate Model's Calculation for Validating the Simplified Model

Below are the algebraic calculations going through the accurate model's equations for calculating $V_{ref,new}$ during switching of the largest capacitor.

$$\begin{aligned}(V'_{ref} - V'_{out}) &= V_{ref}\left[\frac{\left(\frac{(1-z)C_aC_{ref}}{C_{ref}+(1-z)C_a}\right)}{\left(zC_a + \frac{(1-z)C_aC_{ref}}{C_{ref}+(1-z)C_a}\right)}\right] \\ &= V_{ref}\left[\frac{(1-z)C_aC_{ref}}{zC_aC_{ref} + z(1-z)C_a^2 + (1-z)C_aC_{ref}}\right] \\ &= V_{ref}\frac{1-z}{1+z(1-z)\frac{C_a}{C_{ref}}}\end{aligned} \tag{B.0.1}$$

$$\begin{aligned}\Delta V &= (V_{ref} - V_{out}) - (V'_{ref} - V'_{out}) \\ &= V_{ref} - V_{ref}\frac{1-z}{1+z(1-z)\frac{C_a}{C_{ref}}} \\ &= V_{ref}\frac{z + z(1-z)\frac{C_a}{C_{ref}}}{1+z(1-z)\frac{C_a}{C_{ref}}}\end{aligned} \tag{B.0.2}$$

$$
\begin{aligned}
\Delta V_{ref,z} &= \Delta V\left(\frac{(1-x'-z)C_a}{C_{ref}+(1-x'-z)C_a}\right) \\
&= V_{ref}\left(\frac{z+z(1-z)\frac{C_a}{C_{ref}}}{1+z(1-z)\frac{C_a}{C_{ref}}}\right)\left(\frac{(1-z)C_a}{C_{ref}+(1-z)C_a}\right) \\
&= V_{ref}\left(\frac{\frac{z}{C_{ref}}[C_{ref}+(1-z)C_a]}{1+z(1-z)\frac{C_a}{C_{ref}}}\right)\left(\frac{(1-z)C_a}{C_{ref}+(1-z)C_a}\right) \\
&= \frac{z(1-z)\frac{C_a}{C_{ref}}}{1+z(1-z)\frac{C_a}{C_{ref}}}
\end{aligned}
\tag{B.0.3}
$$

$$
\begin{aligned}
V_{ref,new} &= V_{ref} - \Delta V_{ref,z} \\
&= V_{ref}\left(1-\frac{z(1-z)\frac{C_a}{C_{ref}}}{1+z(1-z)\frac{C_a}{C_{ref}}}\right) \\
V_{ref,new} &= V_{ref}\left(\frac{1}{1+z(1-z)\frac{C_a}{C_{ref}}}\right)
\end{aligned}
\tag{B.0.4}
$$

Appendix C

AD7276 Data Sheet

The full data sheet is accessible at: http://www.analog.com/static/imported-files/data_sheets/AD7276_7277_7278.pdf

3 MSPS, 12-/10-/8-Bit ADCs in 6-Lead TSOT

AD7276/AD7277/AD7278

FEATURES

Throughput rate: 3 MSPS
Specified for V_{DD} of 2.35 V to 3.6 V
Power consumption
12.6 mW at 3 MSPS with 3 V supplies
Wide input bandwidth
70 dB SNR at 1 MHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface
SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
Temperature range: −40°C to +125°C
Power-down mode: 0.1 µA typical
6-lead TSOT package
8-lead MSOP package
AD7476 and AD7476A pin-compatible

GENERAL DESCRIPTION

The AD7276/AD7277/AD7278 are 12-/10-/8-bit, high speed, low power, successive approximation analog-to-digital converters (ADCs), respectively. The parts operate from a single 2.35 V to 3.6 V power supply and feature throughput rates of up to 3 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 55 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7276/AD7277/AD7278 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from VDD. This allows the widest dynamic input range to the ADC; therefore, the analog input range for the part is 0 to VDD. The conversion rate is determined by the SCLK.

FUNCTIONAL BLOCK DIAGRAM

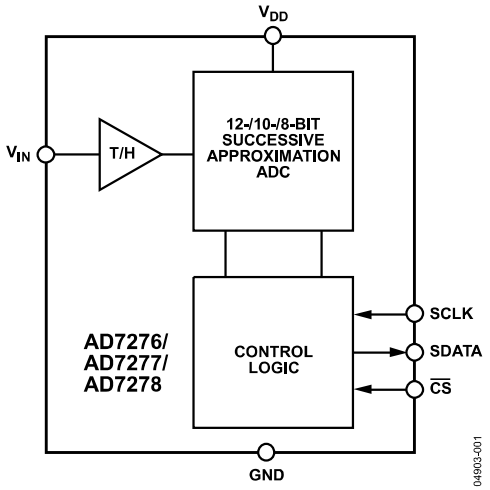


Figure 1.

Table 1.

Part Number	Resolution	Package	
AD7276	12	8-Lead MSOP	6-Lead TSOT
AD7277	10	8-Lead MSOP	6-Lead TSOT
AD7278	8	8-Lead MSOP	6-Lead TSOT
AD7274[1]	12	8-Lead MSOP	8-Lead TSOT
AD7273[1]	10	8-Lead MSOP	8-Lead TSOT

[1] Part contains external reference pin.

PRODUCT HIGHLIGHTS

1. 3 MSPS ADCs in a 6-lead TSOT package.
2. AD7476/AD7477/AD7478 and AD7476A/AD7477A/AD7478A pin-compatible.
3. High throughput with low power consumption.
4. Flexible power/serial clock speed management. This allows maximum power efficiency at low throughput rates.
5. Reference derived from the power supply.
6. No pipeline delay. The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

Rev. C
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SPECIFICATIONS

AD7276 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, B Grade and A Grade: f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, Y Grade:[1] f_{SCLK} = 16 MHz, f_{SAMPLE} = 1 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade[2, 3]	B, Y Grade[2,3]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 1 MHz sine wave, B Grade
				f_{IN} = 100 kHz sine wave, Y Grade
Signal-to-Noise + Distortion (SINAD)[4]	68	68	dB min	
Signal-to-Noise Ratio (SNR)	69	69	dB min	
	70	70	dB typ	
Total Harmonic Distortion (THD)[4]	−73	−73	dB max	
	−78	−78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[4]	−80	−80	dB typ	
Intermodulation Distortion (IMD)[4]				
Second-Order Terms	−82	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−82	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	5	ns typ	
Aperture Jitter	18	18	ps typ	
Full Power Bandwidth	55	55	MHz typ	@ 3 dB
	8	8	MHz typ	@ 0.1 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity[4]	±1.5	±1	LSB max	
Differential Nonlinearity[4]	+1/−0.99	+1/−0.99	LSB max	Guaranteed no missed codes to 12 bits
Offset Error[4]	±4	±3	LSB max	
Gain Error[4]	±3.5	±3.5	LSB max	
Total Unadjusted Error[4] (TUE)	±5	±3.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	µA max	−40°C to +85°C
	±5.5	±5.5	µA max	85°C to 125°C
Input Capacitance	42	42	pF typ	When in track
	10	10	pF typ	When in hold
LOGIC INPUTS				
Input High Voltage, V_{INH}	1.7	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.7	0.7	V max	2.35 V ≤ V_{DD} ≤ 2.7 V
	0.8	0.8	V max	2.7 V < V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[5]	2	2	pF typ	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	±2.5	µA max	
Floating-State Output Capacitance[5]	4.5	4.5	pF typ	
Output Coding	Straight (natural) binary			

Parameter	A Grade[2, 3]	B, Y Grade[2,3]	Unit	Test Conditions/Comments
CONVERSION RATE				
Conversion Time	291	291	ns max	14 SCLK cycles with SCLK at 48 MHz, B Grade
	875	875	ns max	14 SCLK cycles with SCLK at 16 MHz, Y Grade
Track-and-Hold Acquisition Time[4]	60	60	ns min	
Throughput Rate	3	3	MSPS max	See the Serial Interface section
POWER REQUIREMENTS				
V_{DD}	2.35/3.6	2.35/3.6	V min/max	
I_{DD}				Digital I/Ps 0 V or V_{DD}
Normal Mode (Static)	1	1	mA typ	V_{DD} = 3.6 V, SCLK on or off
Normal Mode (Operational)	5.5	5.5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS, B Grade
	2.5	2.5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 1 MSPS, Y Grade
	4.2	4.2	mA typ	V_{DD} = 3 V, f_{SAMPLE} = 3 MSPS, B Grade
	1.6	1.6	mA typ	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, Y Grade
Partial Power-Down Mode (Static)	34	34	µA typ	
Full Power-Down Mode (Static)	2	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	10	µA max	85°C to 125°C
Power Dissipation[6]				
Normal Mode (Operational)	19.8	19.8	mW max	V_{DD} = 3.6 V, f_{SAMPLE} = 3 MSPS, B Grade
	9	9	mW max	V_{DD} = 3.6 V, f_{SAMPLE} = 1 MSPS, Y Grade
	12.6	12.6	mW typ	V_{DD} = 3 V, f_{SAMPLE} = 3 MSPS, B Grade
	4.8	4.8	mW typ	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, Y Grade
Partial Power-Down	102	102	µW typ	V_{DD} = 3 V
Full Power-Down	7.2	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Y Grade specifications are guaranteed by characterization.
[2] Temperature range from −40°C to +125°C.
[3] Typical specifications are tested with V_{DD} = 3 V and at 25°C.
[4] See the Terminology section.
[5] Guaranteed by characterization.
[6] See the Power vs. Throughput Rate section.

Parameter	A Grade[1, 2]	B Grade[1, 2]	Unit	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	2.35/3.6	2.35/3.6	V min/max	
I_{DD}				Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	0.5	0.5	mA typ	V_{DD} = 3.6 V, SCLK on or off
Normal Mode (Operational)	5.5	5.5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS
	3.5	3.5	mA typ	V_{DD} = 3 V
Partial Power-Down Mode (Static)	34	34	µA typ	
Full Power-Down Mode (Static)	2	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	10	µA max	+85°C to +125°C
Power Dissipation[5]				
Normal Mode (Operational)	19.8	19.8	mW max	V_{DD} = 3.6 V, f_{SAMPLE} = 3 MSPS
	10.5	10.5	mW typ	V_{DD} = 3 V
Partial Power-Down	102	102	µW typ	V_{DD} = 3 V
Full Power-Down	7.2	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Temperature range from −40°C to +125°C.
[2] Typical specifications are tested with V_{DD} = 3 V and at 25°C.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS—AD7276/AD7277/AD7278

V_{DD} = 2.35 V to 3.6 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 5.

Parameter[2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[3]	500	kHz min[4]	
	48	MHz max	B grade
	16	MHz max	Y grade
$t_{CONVERT}$	14 × t_{SCLK}		AD7276
	12 × t_{SCLK}		AD7277
	10 × t_{SCLK}		AD7278
t_{QUIET}	4	ns min	Minimum quiet time required between the bus relinquish and the start of the next conversion
t_1	3	ns min	Minimum $\overline{CS}$ pulse width
t_2	6	ns min	$\overline{CS}$ to SCLK setup time
t_3[5]	4	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_4[5]	15	ns max	Data access time after SCLK falling edge
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_7[5]	5	ns min	SCLK to data valid hold time
t_8	14	ns max	SCLK falling edge to SDATA three-state
	5	ns min	SCLK falling edge to SDATA three-state
t_9	4.2	ns max	$\overline{CS}$ rising edge to SDATA three-state
$T_{POWER-UP}$[6]	1	µs max	Power-up time from full power-down

[1] Sample tested during initial release to ensure compliance. All timing specifications given are with a 10 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.
[2] Guaranteed by characterization. All input signals are specified with tr = tf = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[3] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[4] Minimum f_{SCLK} at which specifications are guaranteed.
[5] The time required for the output to cross the V_{IH} or V_{IL} voltage.
[6] See the Power-Up Times section.

Appendix D

EVAL-AD7276SDZ Data Sheet

The official full data sheet for the EVAL-AD7276SDZ is accessible at: http://www.analog.com/static/imported-files/user_guides/EVAL-AD7276SDZ_UG-450.pdf

ANALOG DEVICES

EVAL-AD7276SDZ User Guide
UG-450

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD7276, 3 MSPS, 12-Bit ADC

FEATURES

Full featured evaluation board for the AD7276
PC control in conjunction with the system demonstration platform (EVAL-SDP-CB1Z)
PC software for control and data analysis (time and frequency domain)
Standalone capability

EVALUATION KIT CONTENTS

EVAL-AD7276SDZ evaluation board
Evaluation software CD for the AD7276
9 V mains power supply adapter

ADDITIONAL EQUIPMENT NEEDED

EVAL-SDP-CB1Z system demonstration platform, includes a USB cable
Precision analog signal source
SMB cables
PC running Windows XP SP2, Windows Vista, or Windows 7 with USB 2.0 port

ONLINE RESOURCES

Documents
AD7276 data sheet
EVAL-AD7276SDZ user guide
Required Software
EVAL-AD7276SDZ evaluation software

GENERAL DESCRIPTION

The EVAL-AD7276SDZ is a full featured evaluation board that can be used to easily evaluate all features of the AD7276. The AD7276 is a 12-bit, high speed, low power successive approximation ADC. The part operates from a single 2.35 V to 3.6 V power supply and features throughput rates of up to 3 MSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies greater than 55 MHz.

The evaluation board can be controlled via the system demonstration platform (SDP). The EVAL-SDP-CB1Z board allows the evaluation board to be controlled via the USB port of a PC using the AD7276 evaluation software. The EVAL-AD7276SDZ generates all required power supplies on board and supplies power to the EVAL-SDP-CB1Z controller board. On-board components include the following:

AD8022: dual high speed, low noise op amp
ADA4000-1: single, low cost, precision JFET input operational amplifier
AD780: 2.5 V/3.0 V ultrahigh precision band gap voltage reference
ADP1613: step-up PWM dc-to-dc switching converter
ADP1720: 50 mA, high voltage, micropower linear regulator
ADP7104: 20 V, 500 mA, low noise, CMOS LDO
ADM1185: quad voltage monitor and sequencer
ADG3308: low voltage, 1.15 V to 5.5 V, 8-channel bidirectional logic level translator

FUNCTIONAL BLOCK DIAGRAM

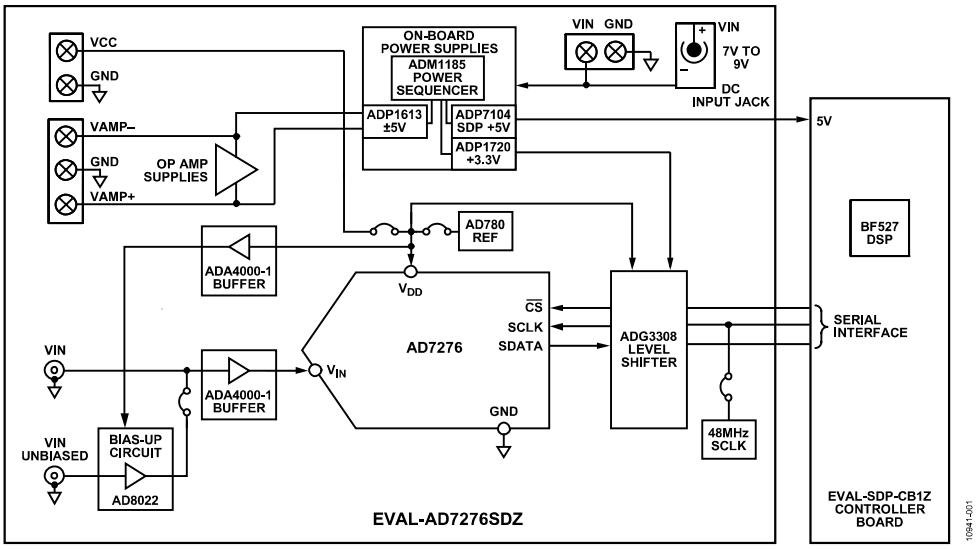


Figure 1.

GETTING STARTED

QUICK START STEPS

To begin using the evaluation board, do the following:

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, install the AD7276 evaluation board software from the CD included in the evaluation board kit. The PC must be restarted after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7276SDZ board as shown in Figure 2. Screw the two boards together using the nylon screw-nut set included in the evaluation board kit to ensure that the boards are connected firmly together.
3. Connect the 9 V power supply adapter included in the evaluation board kit to Connector J1 on the EVAL-AD7276SDZ board.
4. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable. If you are using Windows® XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.
5. Launch the EVAL-AD7276SDZ software from the **Analog Devices** subfolder in the **Programs** menu.

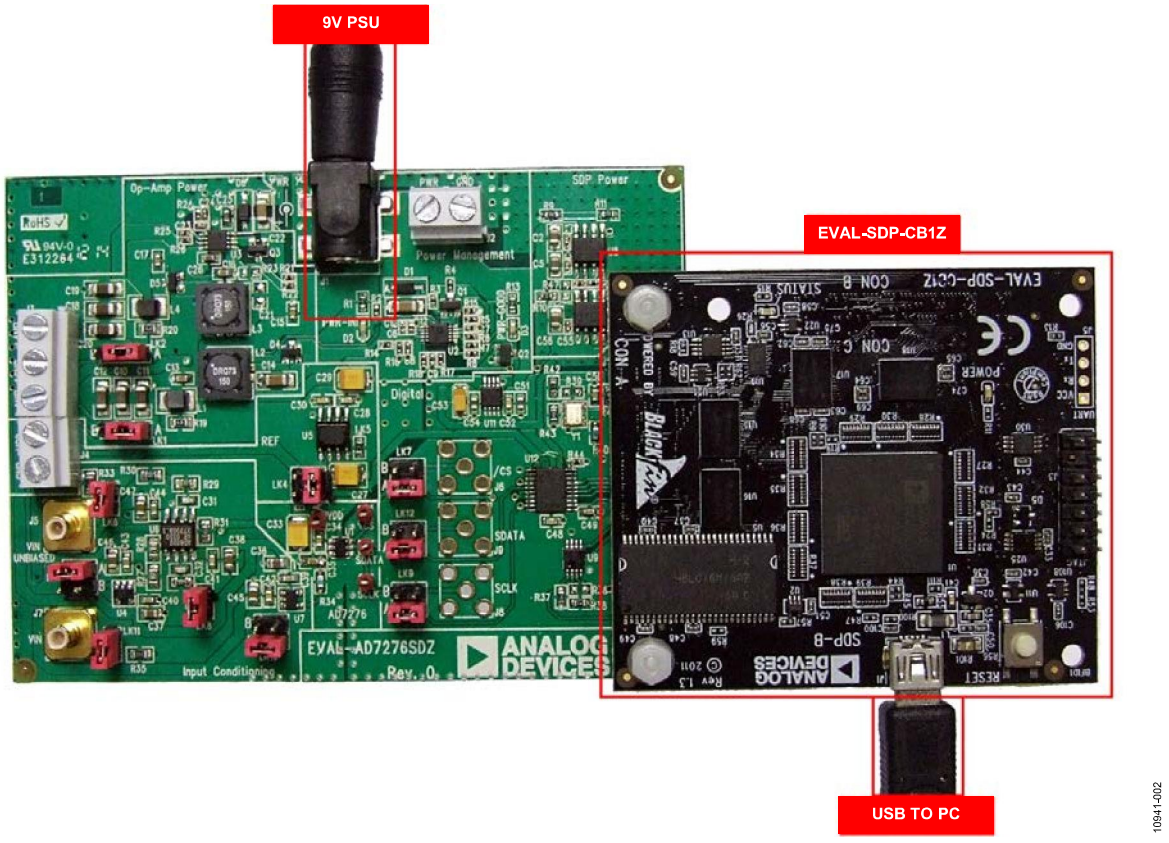


Figure 2. Hardware Configuration—Setting up the EVAL-AD7276SDZ (EVAL-AD7276SDZ on Left and EVAL-SDP-CB1Z on Right)

EVALUATION BOARD SETUP PROCEDURES

The AD7276 evaluation board connects to the EVAL-SDP-CB1Z system demonstration board. The EVAL-SDP-CB1Z board is the controller board, which is the communication link between the PC and the main evaluation board. Figure 2 shows a photograph of the connections made between the AD7276 daughter board and the EVAL-SDP-CB1Z board.

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

1. Connect the EVAL-AD7276SDZ board to Connector A or Connector B of the EVAL-SDP-CB1Z board (see Figure 2).
   a. Screw the two boards together using the nylon screw-nut set included in the evaluation board kit to ensure that the boards are connected firmly together.
2. Connect the 9 V power supply adapter included in the evaluation board kit to Connector J1 of the EVAL-AD7276SDZ board. (Alternatively, a bench power supply can be used to power the EVAL-AD7276SDZ via Connector J2. See Table 1 for more information about the connections and options for the required power supplies.)
3. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable.

EVALUATION BOARD HARDWARE

AD7276 DEVICE DESCRIPTION

The AD7276 can interface to microprocessors or DSPs.

The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7276 uses advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC; therefore, the analog input range for the part is 0 V to V_{DD}. The conversion rate is determined by the SCLK.

For more information about the AD7276, refer to the AD7276 data sheet, which should be used in conjunction with this user guide.

POWER SUPPLIES

The EVAL-AD7276SDZ can be used in two modes: SDP controlled mode and standalone mode (see the Modes of Operation section for more information).

When the EVAL-AD7276SDZ board is used in conjunction with the EVAL-SDP-CB1Z board (SDP controlled mode), connect the ac transformer to Connector J1 on the EVAL-AD7276SDZ board. The V_{DD}, +AMP, and −AMP supplies are generated on board. When the EVAL-AD7276SDZ board is used in standalone mode, the V_{DD} and amplifier supplies must be sourced from external sources (see Table 1).

Alternatively, a bench power supply can be connected to J2 to supply 7 V to 9 V.

Table 1. External Power Supplies Required

Power Supply	Connector	Voltage Range	Purpose
V_{IN} [1]	J1 or J2	7 V to 9 V	Supplies all on-board power supplies, generating all required voltages to run the evaluation board
+AMP	J3-3	+5 V	Supplies the positive rail of the amplifier
−AMP	J3-1	−5 V	Supplies the negative rail of the amplifier
V_{DD}	J4	2.35 V to 3.6 V	Supplies the V_{DD} digital supply

[1] When V_{IN} is supplied, all other power supplies are available on board. If the V_{IN} supply is not used, all other power supplies must be sourced from an external source.

EVALUATION BOARD CIRCUITRY

ANALOG INPUTS

Two analog input options are available for the EVAL-AD7276SDZ:

- VIN (J7)—for use with a unipolar signal source
- VIN UNBIASED (J5)—for use with a bipolar signal source

VIN (J7)

Use the VIN (J7) input when a unipolar signal source is available (see Table 4 for jumper settings). The input is buffered by U7 and fed to the AD7276 via an R-C filter.

Table 4. Unipolar Input Jumper Settings

Link	Jumper Settings
LK8	Removed
All Other Links	Set as described in Table 3.

VIN UNBIASED (J5)

Use the VIN UNBIASED (J5) input when a bipolar signal source is available (see Table 5 for jumper settings). The input is biased up by U6 and buffered by U7 and then is fed to the AD7276 via an R-C filter.

Table 5. Bipolar Input Jumper Settings

Link	Jumper Settings
LK11	Removed
All Other Links	Set as described in Table 3.

REFERENCE OPTIONS

The following on-board reference supply is available:

- AD780: 2.5 V/3.0 V ultrahigh precision band gap voltage reference. The reference is taken from the V_{DD} pin of the AD7276.

Alternatively, an external reference voltage can be applied to J4.

SOCKETS/CONNECTORS

Table 6. Socket/Connector Functions

Socket	Function
J1	PWR. A 7 V to 9 V dc transformer power connector.
J2	A 7 V to 9 V bench supply screw terminal connector.
J3	V_{SS} and V_{DD}. Screw terminal connectors for external amplifier power supplies.
J4	External power supply for V_{DD} of the AD7276.
J5	VIN UNBIASED. Analog input for use with bipolar signal sources.
J6	$\overline{CS}$. External connection to $\overline{CS}$.
J7	VIN. Analog input for use with unipolar signal sources.
J8	SCLK. External connection to SCLK.
J9	SDATA. External connection to SDATA.
J10	EVAL-SDP-CB1Z evaluation board controller socket.

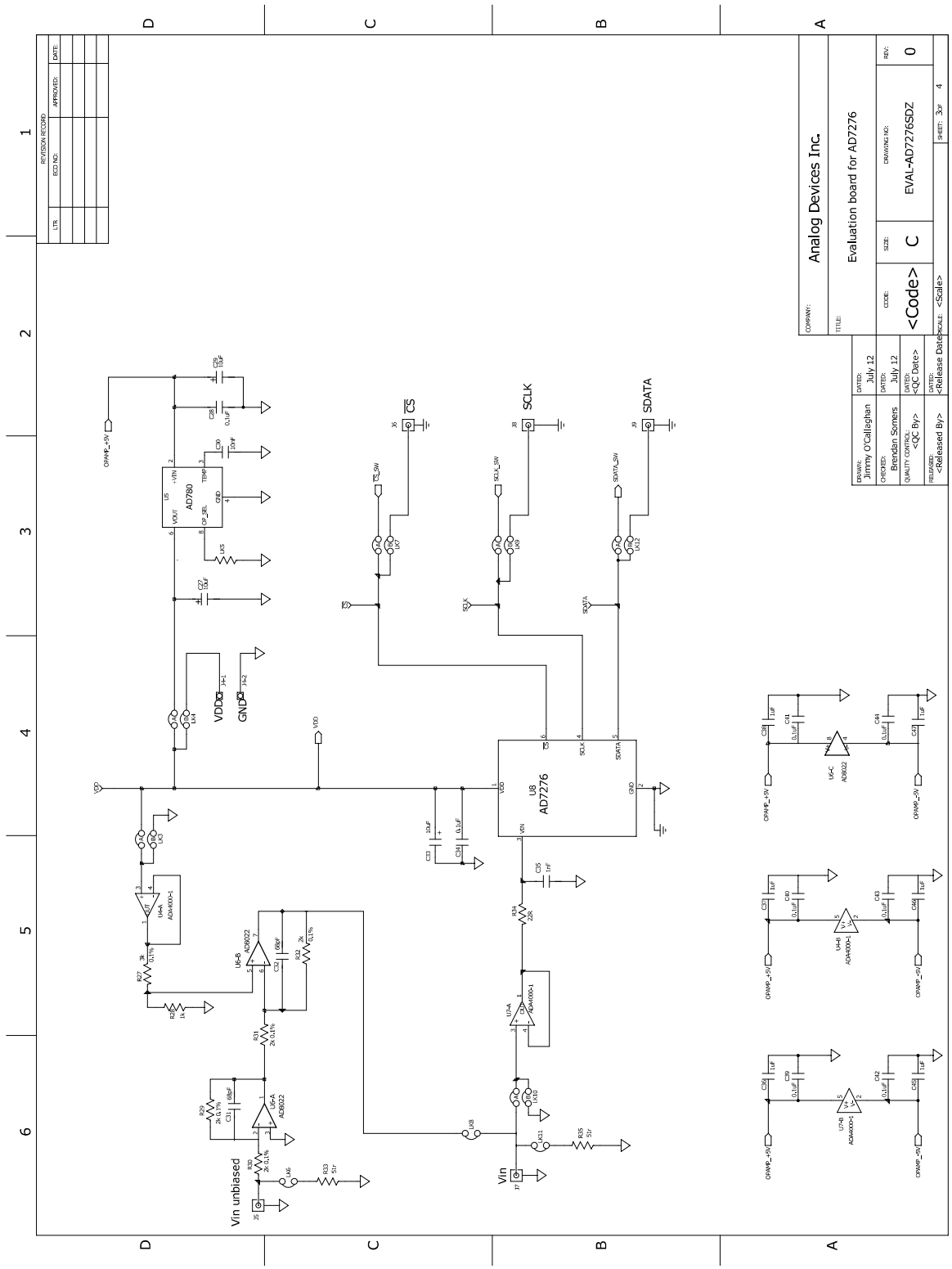


Figure 24. Schematic page 3

Appendix E

EVAL-SDP-CB1Z Data Sheet

The full data sheet is accessible at: http://www.analog.com/static/imported-files/user_guides/SDP_UG_rev1.3.pdf

More information is available at: http://www.analog.com/en/system-demonstration-platform/controller-boards/evaluation/SDP-B/eb.html

PREFACE

Thank you for purchasing the EVAL-SDP-CB1Z System Demonstration Platform (SDP) from Analog Devices, Inc. The SDP is used as part of the evaluation system for many ADI components.

The SDP board is designed to be used in conjunction with various ADI component evaluation boards as part of a customer evaluation environment. The SDP provides USB connectivity through a USB 2.0 high speed connection to the computer allowing users to evaluate components on this platform from a PC application. The SDP is based on ADSP-BF527 Blackfin processor, with the Blackfin processor peripheral communication lines available to the component daughter board through the two identical 120-pin small footprint connectors

Product Overview

The board features:

- Analog Devices ADSP-BF527 Blackfin processor
    - Core performance up to 600 MHz
    - 208 -ball CSP-BGA package
    - 24 MHz CLKIN oscillator
    - 5 Mb of internal RAM memory

- 32Mb flash memory
    - Numonyx M29W320EB or
    - Numonyx M25P32
- SDRAM memory
    - Micron MT48LC16M16A2P-6A - 16 Mb x 16 bits (256 Mb/32 MB)
- 2 x 120-pin small foot print connectors
    - Hirose FX8 -120P-SV1(91),120 Pin Header
- Blackfin processor peripherals exposed
    - SPI
    - SPORT
    - TWI/I^2C
    - GPIO
    - PPI
    - Asynchronous Parallel

For more information, go to http://www.analog.com/sdp.

Purpose of This Manual

The *SDP User Guide* provides instructions for installing the SDP hardware (EVAL-SDP-CB1Z board) and software onto your computer. The necessary installation files are provided with the evaluation daughter board package.

Intended Audience

The primary audience for this manual is a system engineer who seeks to understand how to set up the SDP board and begin USB communications to the computer.

Manual Contents

The manual consists of:

- Chapter 1, "Getting Started" on page 1-1
  Provides software and hardware installation procedure, PC system requirements and basic board information.
- Chapter 2, "Hardware Description" on page 2-1
  Provides information on the EVAL-SDP-CB1Z components.
- Chapter 3, "Schematic" on page 3-1
  Provides EVAL-SDP-CB1Z schematics.

What's New in This Manual

Revision 1.3 of the SDP User Guide revises the document's name to "System Demonstration Platform User Guide".

Appendix F

R&S SMA100A Data Sheet

The full data sheet is accessible at: http://cdn.rohde-schwarz.com/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/SMA100A_dat-sw_en_5213-6412-22_v0700.pdf

Specifications

Specification is only valid for instruments with serial number > 112000.

RF performance

Frequency

Range	R&S®SMA-B103/-B103L	9 kHz to 3 GHz
	R&S®SMA-B106/-B106L	9 kHz to 6 GHz
Resolution of setting		0.01 Hz
Resolution of synthesis	fundamental frequency range 750 MHz to 1500 MHz	
	standard	5 µHz (nom.)
	with R&S®SMA-B22 option	0.2 µHz (nom.)
Setting time	to within < 1 × 10^{-7} for f > 6.6 MHz or < 35 Hz for f < 6.6 MHz no relay switchover, PLL bandwdith normal	
	after IEC/IEEE bus delimiter	< 1.2 ms
	in ALC OFF S&H mode	< 5 ms
	after trigger pulse in List mode or Fast Hopping mode	< 450 µs
Resolution of phase offset setting		adjustable in 0.1° steps
Main PLL bandwith settings	with R&S®SMA-B22 option	
	f ≤ 3 GHz	normal, narrow
	f > 3 GHz	normal
Multiplier for phase-continuous frequency setting	f ≤ 6.6 MHz	rm = 1/2
	6.6 MHz < f ≤ 11.71875 MHz	rm = 1/128
	11.71875 MHz < f ≤ 23.4375 MHz	rm = 1/64
	23.4375 MHz < f ≤ 46.875 MHz	rm = 1/32
	46.875 MHz < f ≤ 93.75 MHz	rm = 1/16
	93.75 MHz < f ≤ 187.5 MHz	rm = 1/8
	187.5 MHz < f ≤ 375 MHz	rm = 1/4
	375 MHz < f ≤ 750 MHz	rm = 1/2
	750 MHz < f ≤ 1500 MHz	rm = 1
	1500 MHz < f ≤ 3 GHz	rm = 2
	f > 3 GHz	rm = 4
Phase-continuous frequency setting range		rm × 1 MHz (nom.)
	with R&S®SMA-B22 option	
	narrow mode	rm × 5 MHz
	wide mode	rm × 20 MHz
Max. phase-continuous frequency step		rm × 2 kHz (nom.)
	with R&S®SMA-B22 option	rm × 100 kHz (nom.)

Frequency sweep

Operating mode		digital sweep in discrete steps
Trigger modes	execute sweep continuously with internal trigger source	auto
	execute one full sweep	single
	execute one step	step
	sweep start and stop controlled by external trigger signal	start/stop
Trigger source	internal	timer
	external	external trigger signal (INST TRIG at rear), rotary knob, remote control
Trigger slope	external trigger signal	positive, negative
Sweep range		full frequency range
Sweep shape		sawtooth, triangle
Step size	linear	full frequency range
	logarithmic	0.01 % to 100 % per step
Dwell time setting range		10 ms to 10 s
Dwell time setting resolution		0.1 ms

Reference frequency

Frequency error	at time of calibration in production	< 1×10^{-8}
	with R&S®SMA-B22 option	< 5×10^{-9}
Aging	after 10 days of uninterrupted operation	≤ 1×10^{-9}/day, ≤ 1×10^{-7}/year
	with R&S®SMA-B22 option	≤ 5×10^{-10}/day, ≤ 3×10^{-8}/year
Maximum temperature effect	in temperature range 0 °C to +50 °C	±6×10^{-8}
	with R&S®SMA-B22 option	±6×10^{-9}
Warm-up time	to nominal thermostat temperature	≤ 10 min
Reference frequnecy output		
Connector type	REF OUT on rear panel	BNC female
Output frequency	sine wave	
	instrument set to internal reference	10 MHz
	instrument set to external reference	applied external reference frequency
Output level		2 dBm to 8 dBm
		5 dBm to 7 dBm (typ.)
Source impedance		50 Ω (nom.)
Reference frequency input		
Connector type	REF IN on rear panel	BNC female
Input frequency		5 MHz, 10 MHz or 13 MHz
Min. frequency locking range		±3×10^{-6}
	with R&S®SMA-B22 option	±1.5×10^{-7}
Input level range	level limits	≥ –6 dBm, ≤ 19 dBm
	recommended input level	0 dBm to 19 dBm
Input impedance		50 Ω (nom.)
Input for electronic tuning of internal reference frequency		
Connector type	EXT TUNE on rear panel	BNC female
Sensitivity		0.5×10^{-8}/V to 3×10^{-8}/V 1×10^{-8}/V to 2×10^{-8}/V (typ.)
	with R&S®SMA-B22 option	5×10^{-9}/V to 2×10^{-8}/V 8×10^{-9}/V to 9.5×10^{-9}/V (typ.)
Input voltage		–10 V to +10 V
Input impedance		10 kΩ (nom.)
	with R&S®SMA-B22 option	5 kΩ (nom.)

Level

The R&S®SMA100A has three different modes for level setting:

NORMAL mode: In this mode, the attenuator switches without wear and tear due to the exclusive use of electronic switches. The maximum specified level depends on the set frequency (see table below).

HIGH POWER mode: In this mode, the electronic attenuator is bypassed with mechanical relays for high output power (up to typ. 28 dBm overrange). The relays are not switched over in this mode. The typical minimum level is –11 dBm.

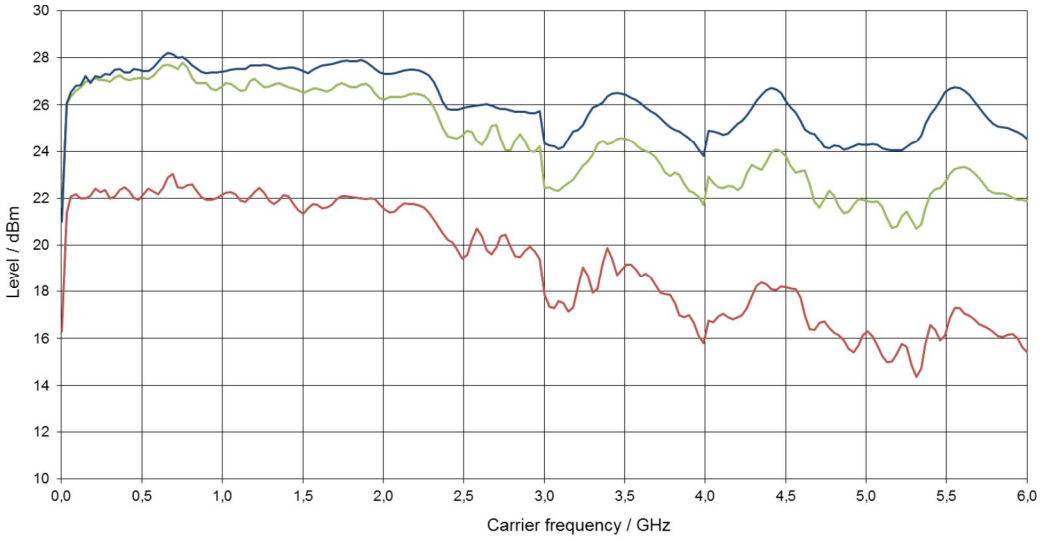
AUTO mode: In this mode, the mechanical relay bypass is switched automatically if the set level is higher than the specified max. level in the NORMAL mode. The output level is specified over the full range from –120 dBm up to +18 dBm (+15 dBm for R&S®SMA-B106).

The R&S®SMA100A is also available without attenuator (R&S®SMA-B103L and R&S®SMA-B106L) options.

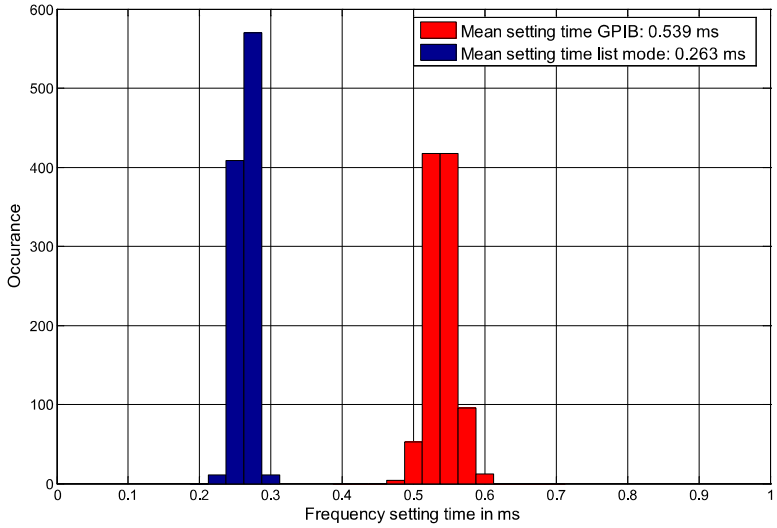
Setting range	with electronic attenuator (R&S®SMA-B103/-B106 option)	–145 dBm to +30 dBm
	without attenuator (R&S®SMA-B103L/-B106L option)	–20 dBm to +30 dBm
Specified level range with R&S®SMA-B103/-B106 frequency option	NORMAL mode	
	100 kHz < f ≤ 200 kHz	–120 dBm to +11 dBm (PEP) [1]
	200 kHz < f ≤ 3 GHz	–120 dBm to +13 dBm (PEP)
	f > 3 GHz	–120 dBm to +9 dBm (PEP)
	AUTO mode	
	100 kHz < f ≤ 30 MHz	–120 dBm to +16 dBm (PEP)
	30 MHz < f ≤ 3 GHz	–120 dBm to +18 dBm (PEP)
	f > 3 GHz	–120 dBm to +15 dBm (PEP)

[1] PEP = peak envelope power.

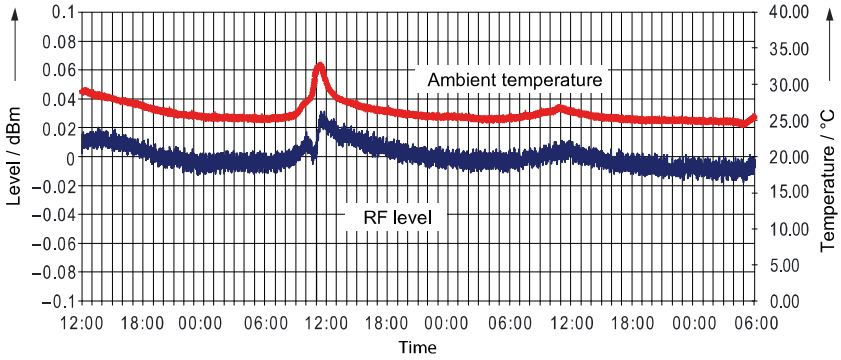
Specified level range with R&S®SMA-B103L/-B106L frequency option	AUTO mode	
	100 kHz < f ≤ 30 MHz	+12 dBm to +17 dBm (PEP)
	30 MHz < f ≤ 3 GHz	+12 dBm to +19 dBm (PEP)
	f > 3 GHz	+10 dBm to +17 dBm (PEP)
Resolution of setting		0.01 dB (nom.)
Level error	ALC state ON, attenuator mode AUTO, temperature range +18 °C to +33 °C	
	100 kHz < f ≤ 3 GHz	< 0.5 dB
	f > 3 GHz	< 0.9 dB
Additional level error with ALC OFF S&H	after “search once” and under stable temperature conditions	< 0.3 dB
Output impedance VSWR in 50 Ω system with R&S®SMA-B103/-B106 frequency option	NORMAL mode, ALC state ON	
	6.6 MHz < f ≤ 3 GHz	< 1.65
	f > 3 GHz	< 1.9
	HIGH POWER mode, ALC state ON	
	6.6 MHz < f ≤ 3 GHz	< 1.75
	f > 3 GHz	< 1.9
Output impedance VSWR in 50 Ω system with R&S®SMA-B103L/-B106L frequency option	without attenuator, ALC state ON	
	6.6 MHz < f ≤ 3 GHz	< 1.9
	f > 3 GHz	< 2.3
Setting time	with GUI update stopped, attenuator mode AUTO,temperature range +18 °C to +33 °C	
	to < 0.1 dB deviation from final value, no relay switchover	
	ALC state ON, after IEC/IEEE bus delimiter	< 1.0 ms
	ALC state OFF, after IEC/IEEE bus delimiter	< 5 ms
	in List mode or Fast Hopping mode, after trigger impulse, f > 6.6 MHz	< 450 µs
	to < 0.3 dB deviation from final value,relay switchover in attenuator mode AUTO	
	after IEC/IEEE bus delimiter	< 10 ms
Interruption-free level setting range	with attenuator mode FIXED, ALC state ON	> 20 dB
Reverse power (from 50 Ω source)	maximum permissible RF power in output frequency range of RF path for f > 1 MHz	
	with R&S®SMA-B103/-B106 option	
	1 MHz < f ≤ 3 GHz	50 W
	3 GHz < f < 6 GHz	10 W
	with R&S®SMA-B103L/-B106L option	0.05 W
Maximum permissible DC voltage	with R&S®SMA-B103/-B106 option	50 V
	with R&S®SMA-B103L/-B106L option	5 V



Maximum available power, attenuator mode NORMAL (lower trace) or HIGH POWER (center trace) and without attenuator (upper trace).



Histogram over 1000 frequency setting time measurements with GPIB remote control and List mode.



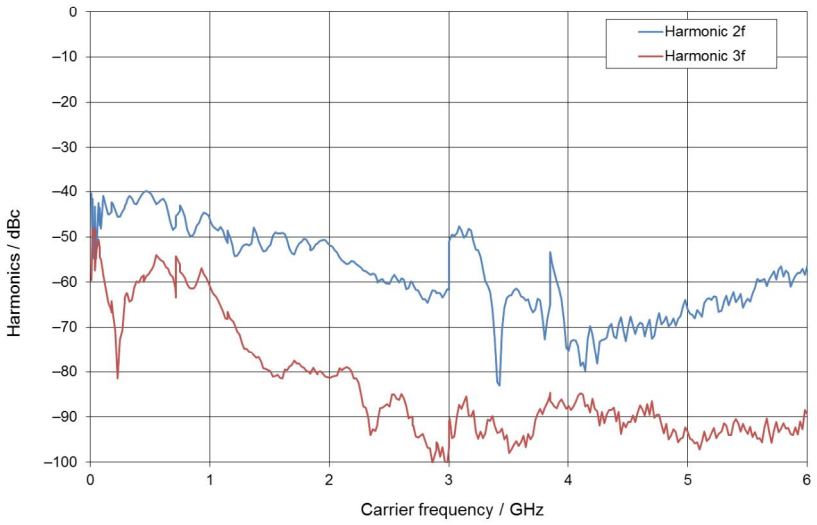
R&S®SMA100A level repeatability at 2.1 GHz, 0 dBm, ALC ON.

Level sweep

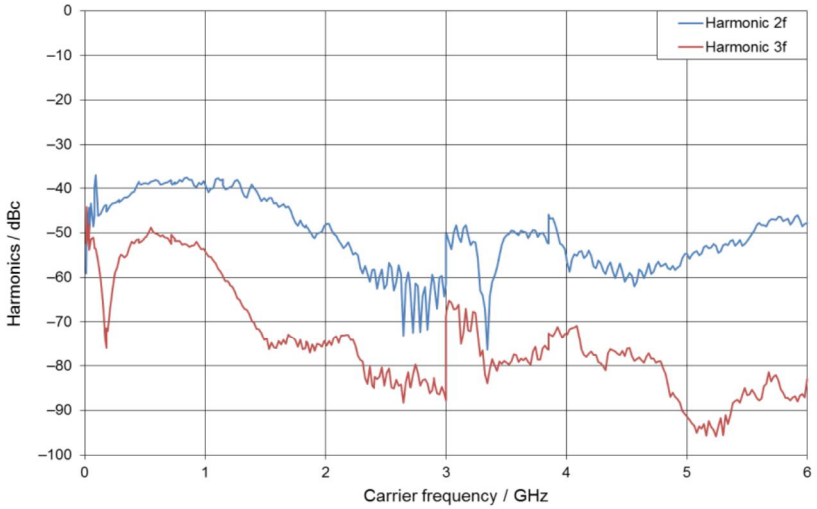
Operating mode		digital sweep in discrete steps
Trigger modes	execute sweep continuously with internal trigger source	auto
	execute one full sweep	single
	execute one step	step
	sweep start and stop controlled by external trigger signal	start/stop
Trigger source	internal	timer
	external	external trigger signal (INST TRIG at rear), rotary knob, remote control
Trigger slope	external trigger signal	positive, negative
Sweep range	with R&S®SMA-B103/-B106 option, attenuator mode AUTO The relay switching threshold (= maximum specified level of attenuator mode NORMAL) must not be exceeded during a sweep.	level range of attenuator modes NORMAL or HIGH POWER
	with R&S®SMA-B103L/-B106L option	full level range
	interruption-free level sweep with attenuator mode FIXED	0.01 dB to 30 dB
Sweep shape		sawtooth, triangle
Step size setting resolution		0.01 dB
Dwell time setting range		10 ms to 10 s
Dwell time setting resolution		0.1 ms

Spectral purity

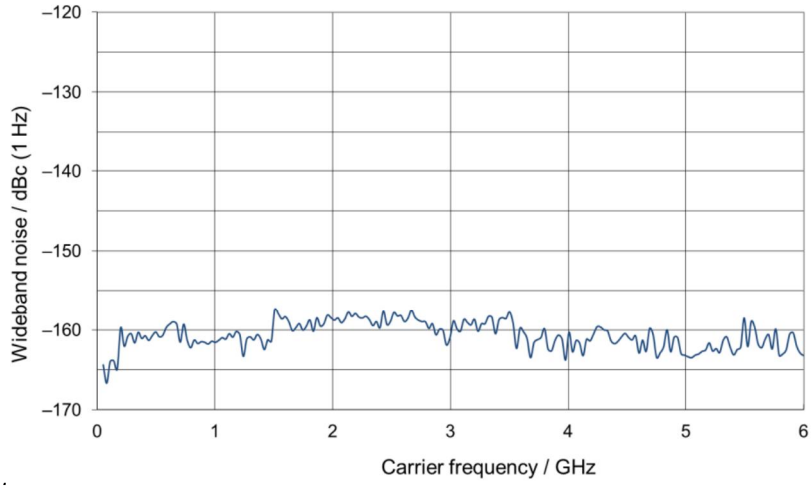
Harmonics	with R&S®SMA-B103/-B106, AUTO/NORMAL mode, CW, level ≤ 9 dBm	
	1 MHz < f ≤ 2 GHz	< –30 dBc
	f > 2 GHz	< –40 dBc
	with R&S®SMA-B103/-B106, HIGH POWER mode, CW, level ≤ 14 dBm with R&S®SMA-B103L/-B106L, CW, level ≤ 15 dBm	
	1 MHz < f ≤ 2 GHz	< –30 dBc
	f > 2 GHz	< –40 dBc
Nonharmonics	CW, level > –10 dBm (with R&S®SMA-B103/-B106), carrier offset > 10 kHz	
	f ≤ 1500 MHz	< –80 dBc
	1500 MHz < f ≤ 3 GHz	< –74 dBc
	f > 3 GHz	< –68 dBc
	CW, level > –10 dBm (with R&S®SMA-B103/-B106), carrier offset > 850 kHz	
	f ≤ 1500 MHz	< –86 dBc
	1500 MHz < f ≤ 3 GHz	< –80 dBc
	f > 3 GHz	< –74 dBc
Nonharmonics with R&S®SMA-B22 option	CW, level > –10 dBm (with R&S®SMA-B103/-B106), carrier offset > 10 kHz PLL bandwdith normal	
	f ≤ 750 MHz	< –96 dBc
	750 MHz < f ≤ 1500 MHz	< –92 dBc
	1500 MHz < f ≤ 3 GHz	< –86 dBc
	f > 3 GHz	< –80 dBc
Subharmonics	f ≤ 1500 MHz	none
	f > 1500 MHz	< –74 dBc
Wideband noise	CW, attenuator mode AUTO, carrier offset > 10 MHz, measurement bandwidth 1 Hz for level > 10 dBm with R&S®SMA-B103L/-B106L for level > 5 dBm with R&S®SMA-B103/-B106	
	9 kHz ≤ f ≤ 6.6 MHz	< –147 dBc
	6.6 MHz < f ≤ 750 MHz	< –152 dBc
	750 MHz < f ≤ 1500 MHz	< –153 dBc
	1.5 GHz < f ≤ 3 GHz	< –150 dBc
	f > 3 GHz	< –148 dBc
SSB phase noise	CW, carrier offset 20 kHz, measurement bandwidth 1 Hz	
	f ≤ 6.6 MHz	–147 dBc (meas.)
	f = 100 MHz	< –147 dBc, –153 dBc (typ.)
	f = 1 GHz	< –131 dBc, –134 dBc (typ.)
	f = 2 GHz	< –125 dBc, –128 dBc (typ.)
	f = 3 GHz	< –121 dBc, –124.5 dBc (typ.)
	f = 4 GHz	< –119 dBc, –121 dBc (typ.)
	f = 6 GHz	< –115 dBc, –118 dBc (typ.)
SSB phase noise with R&S®SMA-B22 option	CW, carrier offset 20 kHz, PLL bandwdith normal, measurement bandwidth 1 Hz	
	f ≤ 6.6 MHz	–152 dBc (meas.)
	f = 100 MHz	< –152 dBc, –157 dBc (typ.)
	f = 1 GHz	< –137 dBc, –141 dBc (typ.)
	f = 2 GHz	< –131 dBc, –134.5 dBc (typ.)
	f = 3 GHz	< –127 dBc, –133 dBc (typ.)
	f = 4 GHz	< –123 dBc, –127 dBc (typ.)
	f = 6 GHz	< –120 dBc, –124 dBc (typ.)
RMS jitter	f = 1 GHz BW = 1 Hz to 10 MHz	430 fs (430 µUI) (meas.)
	f = 155 MHz BW = 100 Hz to 1.5 MHz	60 fs (9 µUI) (meas.)
	f = 622 MHz BW = 1 kHz to 5 MHz	36 fs (22 µUI) (meas.)
	f = 2.488 GHz BW = 5 kHz to 15 MHz	22 fs (55 µUI) (meas.)
RMS jitter with R&S®SMA-B22 option	PLL bandwdith normal	
	f = 1 GHz BW = 1 Hz to 10 MHz	62 fs (62 µUI) (meas.)
	f = 155 MHz BW = 100 Hz to 1.5 MHz	22 fs (3.5 µUI) (meas.)
	f = 622 MHz BW = 1 kHz to 5 MHz	19.5 fs (12 µUI) (meas.)
	f = 2.488 GHz BW = 5 kHz to 15 MHz	18 fs (47 µUI) (meas.)
Residual FM	RMS value at f = 1 GHz	
	0.3 kHz to 3 kHz, weighted (ITU-T)	< 1 Hz
	0.03 kHz to 23 kHz	< 4 Hz
Residual AM	level = 0 dBm RMS value (0.03 kHz to 20 kHz)	< 0.02 %



Measured harmonics at +9 dBm versus carrier frequency (level mode AUTO).



Measured harmonics at +18 dBm versus carrier frequency (level mode AUTO)



Wideband noise at 40 MHz offset and +9 dBm versus carrier frequency measured with the R&S®FSQ8 signal and spectrum analyzer.

Appendix G

KR 2827 Data Sheet

The full data sheet is accessible at: https://krfilters.com/filter-docs/2827.pdf

KR Electronics

General Description

KR 2827 is a 350 KHz lowpass filter. The filter has a minimum 1.5 dB bandwidth of 350 KHz and greater than 30 dB at 400 KHz. Other passband frequencies are available. Please consult the factory.

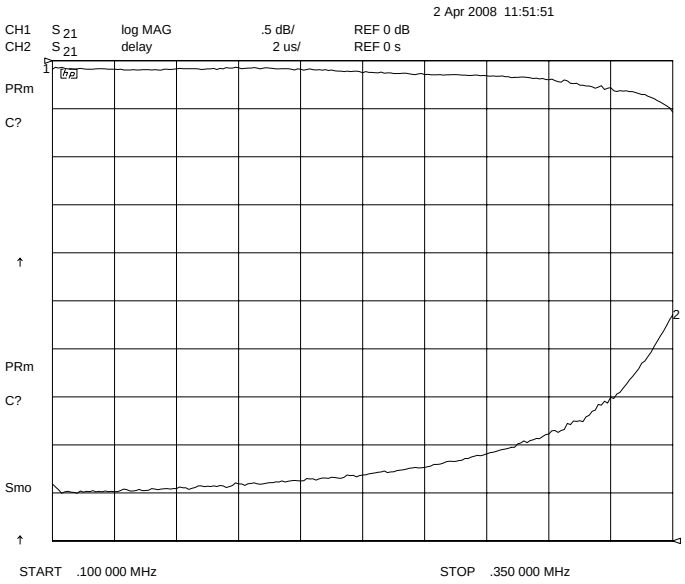
Features

- 350 KHz Lowpass
- SMA Connectors
- 50 Ω Source and Load

Typical Performance

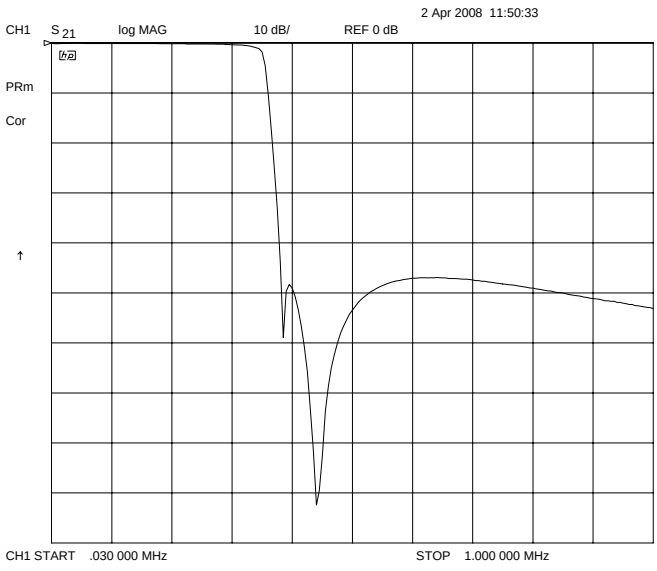
Passband Amplitude & Group Delay

(0.5 dB/div & 2 usec/div)



Overall Response

(10 dB/div)



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Appendix H

Complete Non-Ideal SAR-ADC Simulated Model

```
1
2  function [ Out ] = NonIdealSARADC( Vin , Cr_input )
3
4      vin = Vin + 1/2^13;
5
6      [R,C] = size(vin); % Determine the number of Rows and Columns
7      Out = zeros(R,C); % Stuff the output with zeros
8
9      %assumed total internal capacitance
10     Cap = 0.85*714e-15 * 2^12;
11
12     %Reference capacitance is total capacitance on the line + added
13     %reference capacitor
14      Cr = 1.35*1.2e-7 + Cr_input;
15
16     Vref = 1;
17
18
19
20
21 for r = 1:R
22     for c = 1:C
23     b = zeros(1,12);
24     y=0;
25     x=0;
26         for i=1:12
```

```
27              %move next capacitors from bottom to top
28              z = 1/2^i;
29
30              %Charge drawn from the course after switching
31              %Q(k,i) = (y*(x-y)+z*(1-x+y-z))*Cap*Vref;
32
33              %Equivalent capacitance looking into array from Vref
34              %Ceq = (x-y+z)*(1-x+y-z)*Cap;
35
36
37              %Vref new after charge sharing between Cr and Capacitive array
38               Vref = (1-(y*(x-y)+z*(1-x+y-z))*Cap/Cr)*Vref;
39
40              Vdac = (x-y+z)*Vref;
41
42              x = x-y+z;
43              if vin(r,c) < Vdac
44                  b(i) = 0;
45                  y = z;
46              else
47                  b(i)=1;
48                  y=0;
49              end
50          end
51
52
53      %Output decimal representation of code
54      Out(r,c) = r_bin2dec(b);
55
56
57      %Vref is restored between samples
58
59      Vref = 1;
60
61
62      end
63   end
64
65  end
```

Appendix I

Generating Characteristic Plots

```
function FFT_out = GenerateCharacteristics( )

fs = 2823500;
N =12;

    L = 2^14;
    %Identify Four Input Frequencies
    fin(1) = fs/L*1201; % ¬207725.605
    fin(2) = fs/L*1423; % ¬244561.733
    fin(3) = fs/L*1657; % ¬284973.767
    fin(4) = fs/L*1901; % ¬326850.628

     %L = 2^17;
     %%Identify Four Input Frequencies
     %fin(1) = fs/L*9643; % ¬207725.605
     %fin(2) = fs/L*11353; % ¬244561.733
     %fin(3) = fs/L*13229; % ¬284973.767
     %fin(4) = fs/L*15173; % ¬326850.628

    %Scale samplitude to match measured data
    vpkpk(1) = 2834.417/2^12/2;
    vpkpk(2) = 2772.545/2^12/2;
    vpkpk(3) = 2739.636/2^12/2;
    vpkpk(4) = 2638.545/2^12/2;

    %Select Capacitor
    Cr_input(1) = 0; %% no cap
    Cr_input(2) = 1.00E-10 ;
    Cr_input(3) = 1.00E-9 ;
```

```
30      Cr_input(4) = 2.20E-9 ;
31      Cr_input(5) = 4.70E-9 ;
32      Cr_input(6) = 1.00E-8 ;
33      Cr_input(7) = 2.20E-08 ;
34      Cr_input(8) = 4.70E-08 ;
35      Cr_input(9) = 1e-7;
36      Cr_input(10) = 2.20E-07 ;
37      Cr_input(11) = 4.70E-07 ;
38      Cr_input(12) = 1E-06 ;
39      Cr_input(13) = 2.20E-06 ;
40      Cr_input(14) = 4.70E-06  ;
41      Cr_input(15) = 1.00E-05;
42      Cr_input(16) = 2.20E-05;
43      Cr_input(17) = 4.70E-05;
44      Cr_input(18) = 1.00E-04;
45      Cra = Cr_input;
46
47      %Initialize empty arrays
48      SFDR_c=zeros(size(fin,2),size(Cra,2),1);
49      SNDR_c=zeros(size(fin,2),size(Cra,2),1);
50      SNR_c=zeros(size(fin,2),size(Cra,2),1);
51      THD_c=zeros(size(fin,2),size(Cra,2),1);
52      SINAD_c=zeros(size(fin,2),size(Cra,2),1);
53      H2_c=zeros(size(fin,2),size(Cra,2),1);
54      H3_c=zeros(size(fin,2),size(Cra,2),1);
55
56
57      time = linspace(0 , 1/fs*(L-1), L); % Set the time base for the samples
58      V_peak = 1; % Set the peak voltage of the sine wave.
59      %u = zeros(5,L);
60
61
62
63
64  for j=1:size(fin,2)
65
66      %Add signal & harmonics
67      u = zeros(5,L);
68      u(5,:) = (sin(5*2*pi*fin(j)*time));
69      u(4,:) = (sin(4*2*pi*fin(j)*time));
70      u(3,:) = (sin(3*2*pi*fin(j)*time));
71      u(2,:) = (sin(2*2*pi*fin(j)*time));
72      u(1,:) = (sin(1*2*pi*fin(j)*time));
73
74      %Only signal is used for this model
```

```
75      samples = u(1,:);
76
77      %initialize size of noise samples needed
78      noise_size = size(samples);
79
80      %scale sample and add noise to input
81      scaled_samples = samples*vpkpk(j)+0.5+ 5e-5*rand(noise_size) - ...
            5e-5*rand(noise_size);
82
83
84      %Re-Initialize arrays
85      SFDR = zeros(size(Cra,2),1);
86      SNDR = zeros(size(Cra,2),1);
87      THD  = zeros(size(Cra,2),1);
88      SNR   = zeros(size(Cra,2),1);
89      SINAD   = zeros(size(Cra,2),1);
90      H2   = zeros(size(Cra,2),1);
91      H3   = zeros(size(Cra,2),1);
92
93      ND = 45e-5*rand(noise_size) - 45e-5*rand(noise_size) ;
94
95      for i=1:size(Cra,2)
96          %Input scaled samples into the SAR-ADC Model
97          [quantized_samples] = NonIdealSARADC(scaled_samples(:,:), ...
                Cr_input(i));
98          steps = 2^N;
99
100         voltage_samples = V_peak*( 2* quantized_samples/steps);
101
102         % Manually center voltage samples and dd noise distortion
103         voltage_samples = voltage_samples - sum(voltage_samples)/L + ND ;
104
105         % generate an array of the frequencies for the FFT's bins.
106         frequency = fs/2*linspace(0, 1, L/2 + 1);
107         %
108         FFT_out = fft(voltage_samples,L)/L;
109
110         fftdata = 2*abs(FFT_out(1:(L/2+1)));
111
112         [SNDR(i) , THD(i), SNR(i), SFDR(i), SINAD(i), H2(i), H3(i)] = ...
                Analyse2(fftdata,0);
113
114         if i==0 && j == 0
115
116         end
```

```
117
118         fprintf(' %d Hz : %d F \n',fin(j),Cr_input(i));
119     end
120
121
122     SNDR_c(j,:) = SNDR;
123     SFDR_c(j,:) = SFDR;
124     SNR_c(j,:) = SNR;
125     THD_c(j,:) = THD;
126     SINAD_c(j,:) = SINAD;
127     H2_c(j,:) = H2;
128     H3_c(j,:) = H3;
129
130
131
132 end
133
134
135 %Plot Characteristic Curves
136
137  greycolors = [0.46 0.46 0.46;  0.80 0.80 0.80; 0.63 0.63 0.63; 0 0 0];
138
139 for i=1:4
140
141 semilogx(Cra,SNDR_c(i,:),'color',greycolors(i,:), 'linewidth', 2);
142
143     hold on;
144 end
145 hold off;
146     title('SNDR vs Reference Capacitance')
147     xlabel('Capacitance (F)')
148     ylabel('SNDR (dB)')
149     legend('207kHz','244kHz','285kHz','327kHz')
150
151 figure(2);
152
153 for i=1:4
154 semilogx(Cra,SFDR_c(i,:),'color',greycolors(i,:), 'linewidth', 2);
155
156      hold on;
157 end
158 hold off
159     title('SFDR vs Reference Capacitance')
160     xlabel('Capacitance (F)')
161     ylabel('SFDR (dB)')
```

```
      legend('207kHz','244kHz','285kHz','327kHz')
      figure(3);

for i=1:4
semilogx(Cra,SNR_c(i,:),'color',greycolors(i,:), 'linewidth', 2);

      hold on;
end
hold off
    title('SNR vs Reference Capacitance')
    xlabel('Capacitance (F)')
    ylabel('SNR (dB)')
     legend('207kHz','244kHz','285kHz','327kHz')
figure(4);
for i=1:4
semilogx(Cra,THD_c(i,:),'color',greycolors(i,:), 'linewidth', 2);

     hold on;
end

hold off
    title('THD vs Reference Capacitance')
    xlabel('Capacitance (F)')
    ylabel('THD (dB)')
     legend('207kHz','244kHz','285kHz','327kHz')

hold off;

end;
```

Appendix J

Finding The Bins of the Harmonics

```
%"data" holds FFT information

    %Identify the size of the FFT
    L = size(data,2);

    %Find Sampling Frequency
    fs = 2*L;

    %First bin is DC
    dc = 1;

    %Set DC to 0, this allows a reliable read for the input signal when ...
       the signal has large DC power
    data(dc) = 0;

    %convert data to decibels
    dB_data = 20*log10(data);

    %find the bin and magnitude of the input signal
    [Va, fa] = max(dB_data(:));

%Find harmonics
    h = 1:10; %find the first 10 harmonics
    % +- Kfs +- nf1
    K=0;
    n = 1;
    % s1 and s2 denote sign
    s1 = 1;
    s2 = 1;
```

```
29      for i=1:20
30          h(i) = s1*K*fs + s2*n*fa;
31          if h(i) > L
32              s1 = 1;
33              K = K+1;
34              s2 = -1;
35          elseif h(i) < 0
36              s1 = -1;
37              s2 = 1;
38          end
39          h(i) = s1*K*fs+s2*n*fa-i+1;
40          n = n+1;
41
42      end
```

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